



Design Example Report

Title	<i>14.35 W High Efficiency TRIAC Dimmable Non-Isolated Tapped-Buck LED Driver Using LYTSwitch™ LYT4311E</i>
Specification	190 VAC – 265 VAC Input; 41 V _{TYP} , 350 mA Output
Application	PAR30 LED Driver
Author	Applications Engineering Department
Document Number	DER-365
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Revision	1.0

Summary and Features

- Single-stage power factor correction combined with constant current (CC) output
- Efficiency ~89% at 230 VAC
- TRIAC dimmable
 - Works with a wide selection of TRIAC dimmers
- Low-cost, low component count, small size PCB
- Fast start-up time (<300 ms) – no perceptible delay
- Integrated protection and reliability features
 - Output short-circuit protected with auto-recovery
 - Auto-recovering thermal shutdown with large hysteresis
 - No damage during brown-out conditions
- PF >0.95 at 230 VAC
- A-THD < 15% at 230 VAC
- Meets EN55015 conducted EMI

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

The document describes a non-isolated, high power factor (PF), high efficiency, TRIAC dimmable LED driver designed to drive a nominal LED string voltage of 41 V at 350 mA from an input voltage range of 190 VAC to 265 VAC (50 Hz typical).

The topology used is a single-stage non-isolated tapped buck that meets high power factor, constant current regulation, and dimming requirements for this design.

This document contains the LED driver specification, schematic, PCB details, bill of materials, transformer documentation and typical performance characteristics.

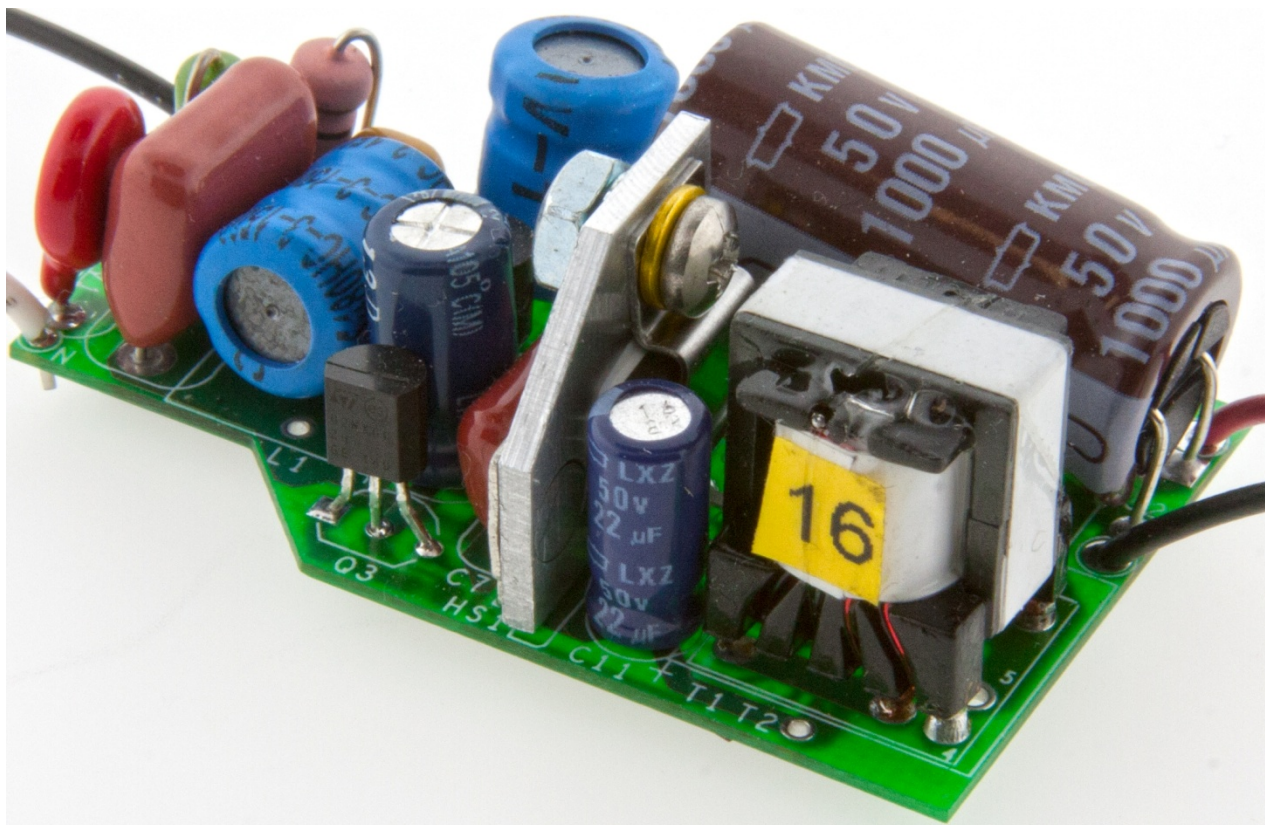


Figure 1 – Populated Circuit Board, Angle View.



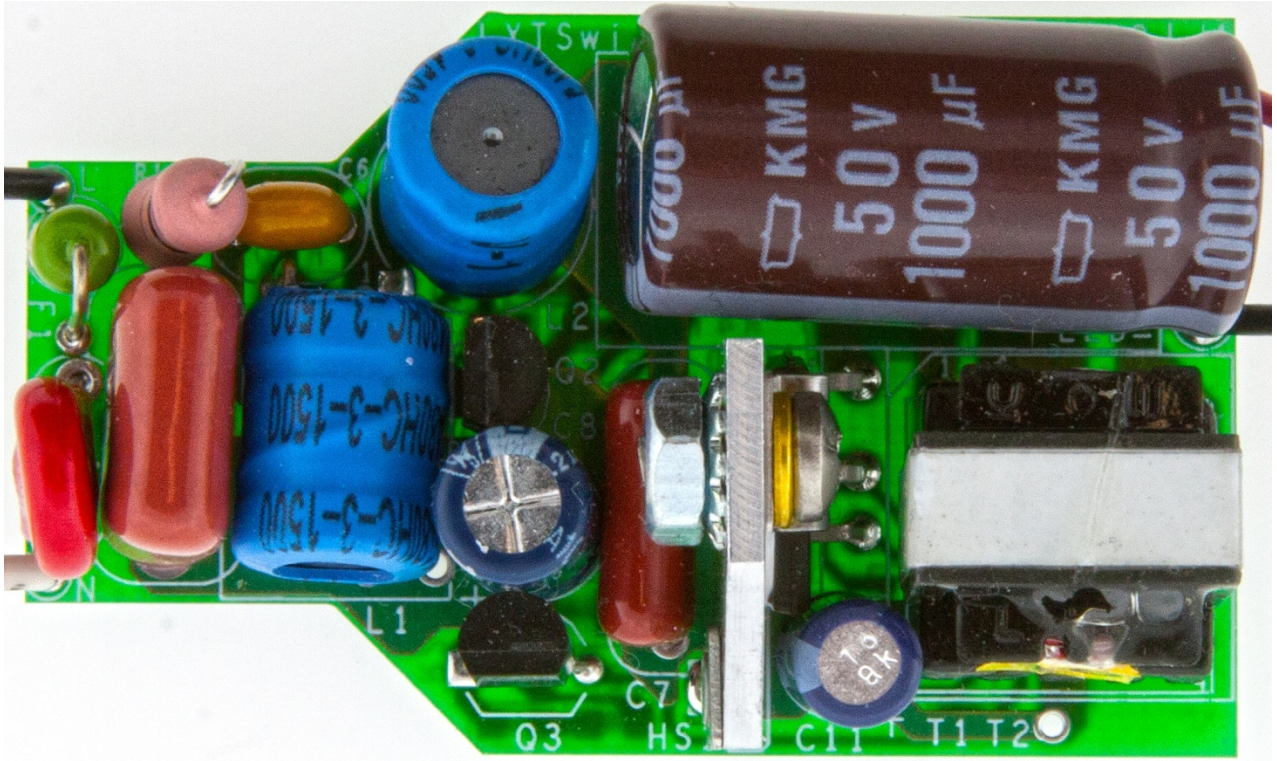


Figure 2 – Populated Circuit Board, Top View.



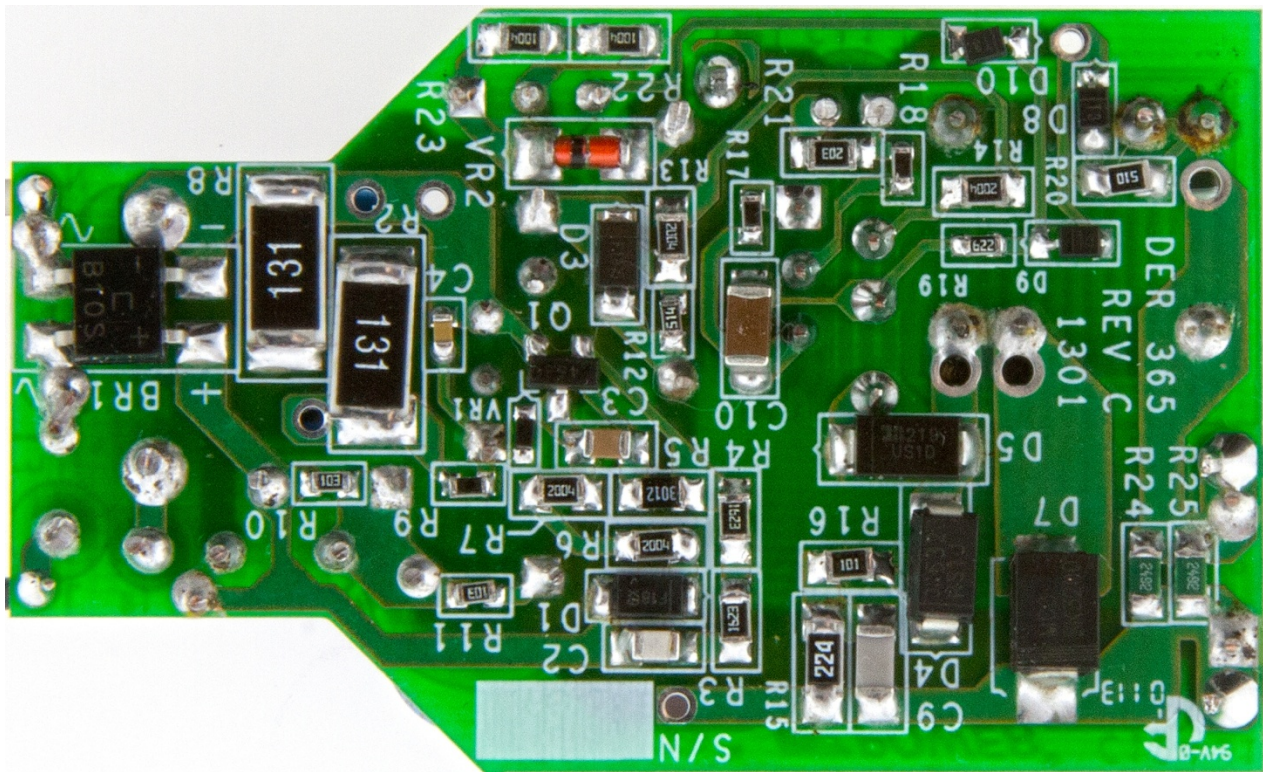


Figure 3 – Populated Circuit Board, Bottom View.



2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input Voltage Frequency	V_{IN} f_{LINE}	190	230 50/60	265	VAC Hz	2 Wire – no P.E.
Output Output Voltage Output Current Total Output Power Continuous Output Power	V_{OUT} I_{OUT} P_{OUT}	38	41 350 14.35	44	V mA W	$V_{OUT} = 41\text{ V}$, $V_{IN} = 230\text{ VAC}$, $25\text{ }^{\circ}\text{C}$
Efficiency Full Load	η	88	89		%	Measured at P_{OUT} $25\text{ }^{\circ}\text{C}$
Environmental Conducted EMI Safety Ring Wave (100 kHz) Differential Mode (L1-L2) Common mode (L1/L2-PE) Differential Surge						CISPR 15B / EN55015B Non-Isolated 2.5 500 kV V
Power Factor		0.95				Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 230 VAC, 50 Hz
Harmonic Currents						EN 61000-3-2 Class C
Ambient Temperature	T_{AMB}				$^{\circ}\text{C}$	



3 Schematic

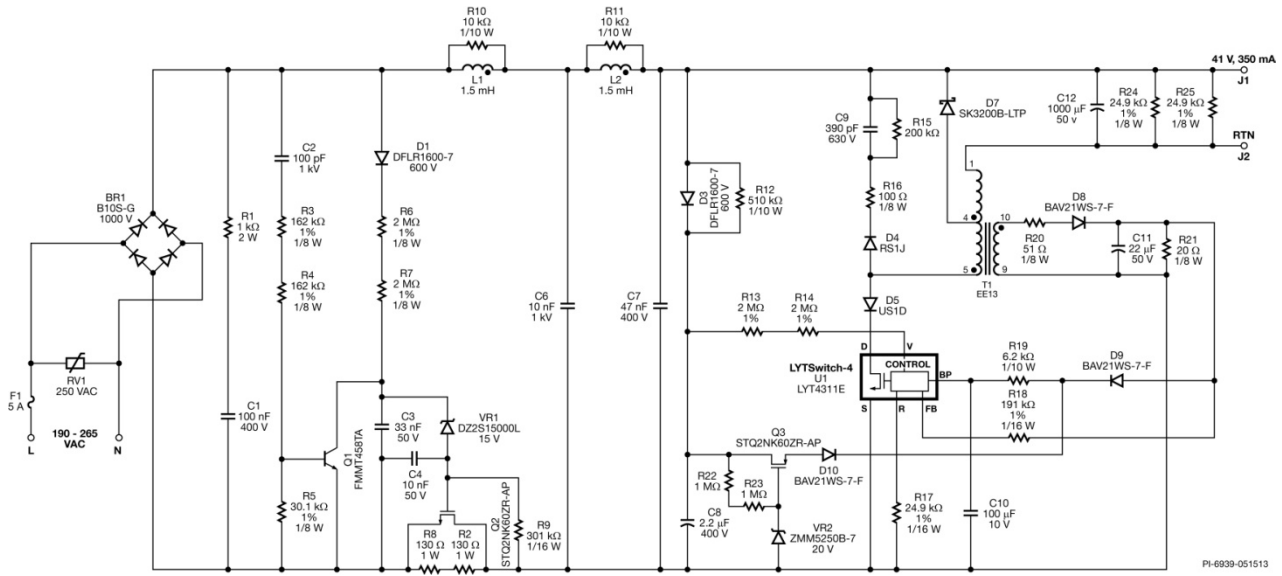


Figure 4 – Schematic.



4 Circuit Description

The LYT4311E (U1) is a highly integrated primary-side controller intended for use in LED driver applications. It provides high power factor while regulating the output current across a range of input (190 VAC to 265 VAC) in a single conversion stage. All of the control circuitry responsible for these functions plus the high-voltage power MOSFET is incorporated into the IC.

4.1 Input EMI Filtering

Fuse F1 provides protection from component failure and RV1 provides a clamp to limit the maximum voltage during differential line surge events. Bridge Rectifier BR1 rectifies the AC line voltage.

EMI filtering is provided by inductors L1, L2, and capacitors C6 and C7. Resistor R10 and R11 across L1 and L2 damp the self-resonance of the inductors to avoid noise peaking in the conducted EMI plot at the resonant frequency of these inductors.

The effect of magnetic coupling between L1 and L2 is carefully considered in the layout in order to yield consistent EMI response since the chosen inductors are not magnetically shielded, are connected in series and adjacent to each other. In this design, L1 is mounted perpendicular to L2 and the start and finish windings are well-controlled and is indicated by a dot on schematic and PCB. (See inductor manufacturer data sheet for information about the start and finish windings)

4.2 Power Circuit

The topology chosen in this design is a low-side tapped buck configured to provide low THD, high power factor, and constant current output for the input voltage range of 190 VAC to 265 VAC.

The tapped buck converter offers the advantage of reduced magnetic component size, reduced current stress on the main switch U1, and reduced voltage stress on the output diode D7. The reduced current stress on the main switch enables the use of a smaller switching device for a more cost effectiveness design. The lower voltage stress on the output diode enables the use of low V_F (Schottky) for improved efficiency.

Inductor T1 is the main inductor of the buck converter. It consists of three windings, primary, secondary, and bias. The ratio is chosen to be 4:1 (primary to secondary ratio) to enable the use of a 200 V output diode while keeping the maximum voltage of U1 LYT4311E well below its maximum value.

Output diode D7 conducts every time U1 is off and transfers energy to the load. Diode D5 is necessary to prevent reverse current from flowing through U1 while the voltage across C7 (rectified input AC) falls below the output voltage. A voltage clamp circuit was also added to limit voltage spike created by the leakage inductance of T1. The voltage clamp network is formed by diode D4, capacitor C9, and resistors R15 and R16.



Output capacitor C12 is chosen to minimize output ripple (<30%). Pre-load resistors R24 and R25 cause the output to quickly discharge below the LED string voltage when the AC is removed and ensuring that the lamp is extinguished rather than there being a slight glow for several seconds after AC is removed.

To provide peak line voltage information to U1, the incoming rectified AC peak charges C8 via D3. This is then fed into the VOLTAGE MONITOR (V) pin of U1 as a current via R13, and R14. Resistor R12 provides discharge path to allow the voltage across C8 to track changes in the incoming AC.

The line overvoltage shutdown function, sensed via the V pin current, extends the rectified line voltage withstand (during surges and line swells) to the 725 BV_{DSS} rating of the internal power MOSFET.

Capacitor C10 provides local decoupling for the BYPASS (BP) pin of U1 which is the supply pin for the internal controller. During start-up, C10 is charged to ~6 V from an internal high-voltage current source connected to the DRAIN (D) pin of U1. Capacitor C10 was chosen to be 100 μ F to enable the device to operate better in deep dimming mode, otherwise 4.7 μ F can be used as LYT4311 has only one power mode.

The REFERENCE (R) pin of U1 is tied to ground (SOURCE) via resistor R17. A 24.9 k Ω value is used to provide tight CC regulation.

4.3 Bias Supply and Output Feedback

A bias winding on T1 is used to provide feedback and supply to the IC. The flyback voltage on the bias winding is rectified by D8 and filtered by C11 to smooth the voltage and R20 to reduce excess voltage coupled from the leakage inductance energy. The feedback current is then fed to the FEEDBACK (FB) pin thru resistor R18. Diode D9 and R19 link the BP pin to the bias winding. Diode D9 is necessary to isolate C10 from C11 during start-up and resistor R19 limits the current supplied to the BP pin from the bias winding. R21 provides load on the bias supply to hasten the discharge of C11 during AC cycle and also helps in achieving higher dim ratio.

4.4 TRIAC Phase Dimming Control Compatibility

The requirement to provide output dimming with low cost, TRIAC based, leading edge and trailing edge phase dimmers introduced a number of trade-offs with the design.

Due to the much lower power consumed by LED based lighting, the current drawn by the lamp is below the holding current of the TRIAC in many dimmers. This causes undesirable behavior such as limited dim range and/or flickering when the TRIAC fires inconsistently. The relatively large impedance presented to the line by the LED could cause significant ringing to occur due to the inrush current charging the input capacitance when the TRIAC turns on. This effect can cause shimmer as the ringing may cause the TRIAC current to fall to zero and turn off.



The damper, bleeder, and linear regulator circuit incorporated in the design overcome these issues with minimal impact on efficiency of the driver.

Resistor R2 and R8 provide passive damping and the surrounding circuit comprised of D1, R6, R7, C3, VR1, C4, Q2, and R9 minimize power dissipation of R2 and R8 by operating Q2 in linear mode approximately 2 ms after the TRIAC turns ON. Capacitor C2, R3, R4, R5 and Q1 provide a discharge path so that Q2 is initially turned OFF when the next TRIAC switching cycle begins. The values were also selected such that when there is no TRIAC connected, Q2 will be permanently ON which helps improve efficiency in non-dimming operation.

The passive bleeder network comprises of capacitor C1 and R1. This network damps the input network and also provides the required latching and holding current for TRIAC dimmers.

The linear regulator circuit R22, R23, VR2, Q3, and D10 were added to keep the supply of the IC (BP pin) constant - allowing it to operate normally at very low conduction angle or with very low input voltage and making the IC act as a load (especially for TRIACs with high leakage current). Most high power rated (>600 W) TRIAC dimmers have an LC input filter. If C is large enough to provide energy to charge the input stage of the LED driver, the LED may turn on as the LED load is energized until the input is discharged. The cycle then repeats and causes flickering of the LED load even if the TRIAC is off.

The linear regulator is not activated when the bias voltage is higher than $V_{ZVR2} + V_{tQ3} + V_{fD10}$. Voltage regulator VR2 is chosen such that the linear regulator will only work during deep dimming when the bias voltage is sufficiently low, to minimize Q3 power dissipation. MOSFET Q3 can be replaced with a BJT (400V) for cost reduction and resistors R22 and R23 must be adjusted accordingly to provide sufficient drive especially when the input voltage is low during deep dimming condition.



5 PCB Layout

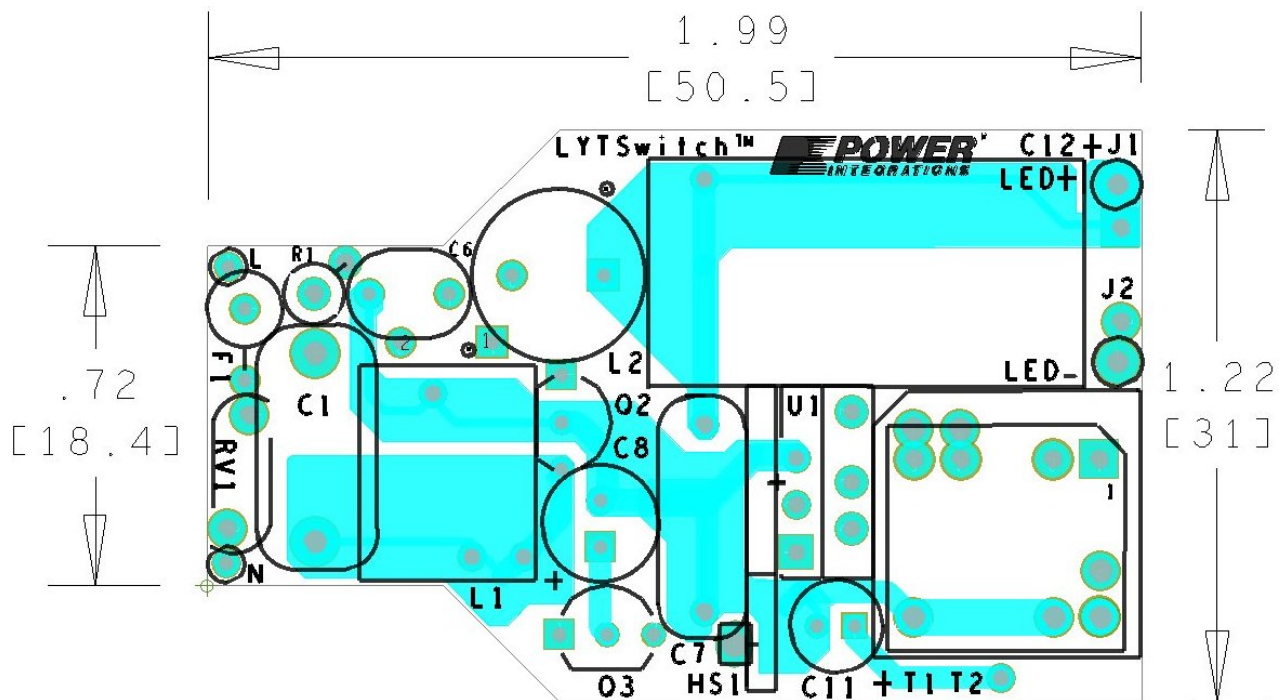


Figure 5 – Top Side.

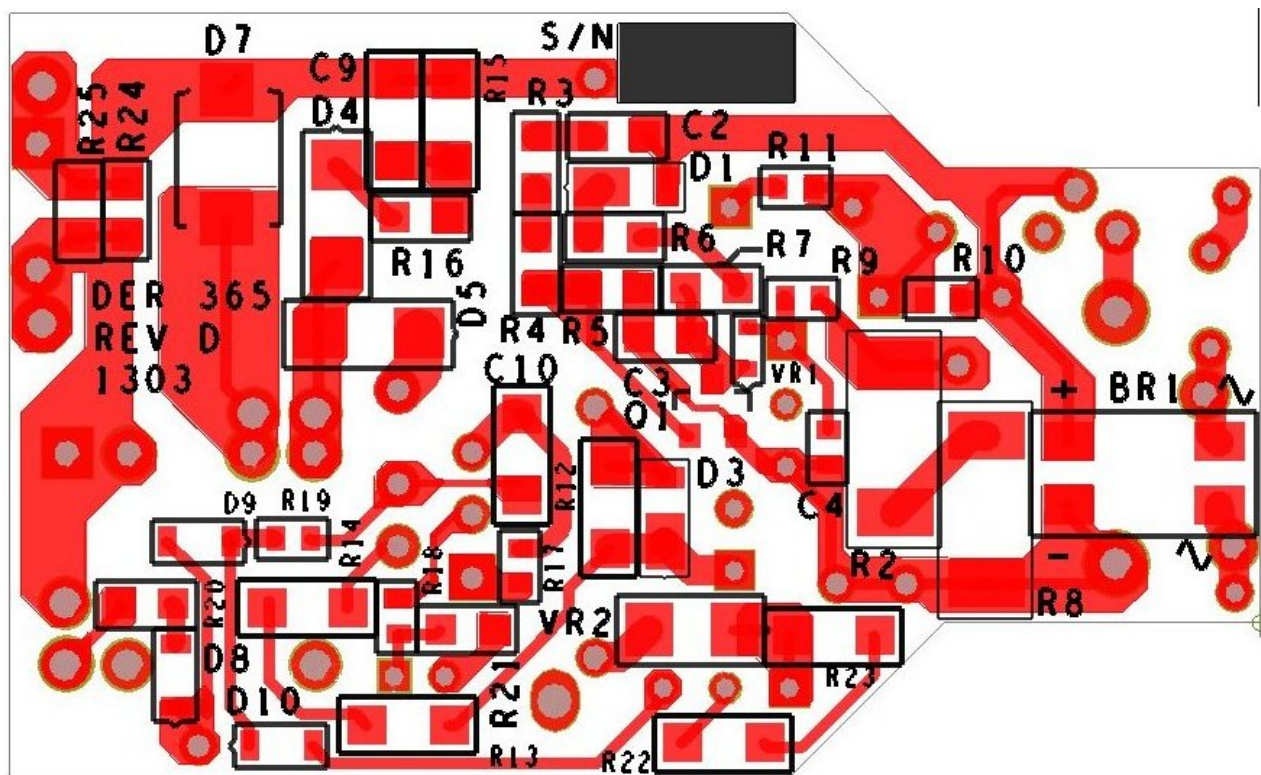


Figure 6 – Bottom Side.



6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip Technology
2	1	C1	100 nF, 400 V, Film	ECQ-E4104KF	Panasonic
3	1	C2	100 pF, 1000 V, Ceramic, NPO, 0805	C0805C101MDGACTU	Kemet
4	1	C3	33 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB333	Yageo
5	1	C4	10 nF 50 V, Ceramic, X7R, 0603	C0603C103K5RACTU	Kemet
6	1	C6	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX
7	1	C7	47 nF, 400 V, Film	ECQ-E4473KF	Panasonic
8	1	C8	2.2 μ F, 400 V, Electrolytic, (6.3 x 11)	TAB2GM2R2E110	Ltec
9	1	C9	390 pF, 630 V, Ceramic, NPO, 1206	C3216C0G2J391J	TDK
10	1	C10	100 μ F, 10 V, Ceramic, X5R, 1206	C3216X5R1A107M	TDK
11	1	C11	22 μ F, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
12	1	C12	1000 μ F, 50 V, Electrolytic, Gen. Purpose, (12.5 x 25)	EKMG500ELL102MK25S	Nippon Chemi-Con
13	2	D1 D3	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
14	1	D4	600 V, 1 A, Fast Recovery, 250 ns, SMA	RS1J-13-F	Diodes, Inc.
15	1	D5	Diode ULTRA FAST, SW, 200 V, 1 A, SMA	US1D-13-F	Diodes, Inc.
16	1	D7	200 V, 3 A, DIODE SCHOTTKY 1 A 200 V, SMB	SK3200B-LTP	Micro Commercial
17	3	D8 D9 D10	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
18	1	F1	5 A, 250 V, Fast, Microfuse, Axial	0263005.MXL	Littlefuse
19	2	L1 L2	1.5 mH, 0.250 A, 10%	RL-5480HC-3-1500	Renco
20	1	Q1	NPN, HP, 400 V, 225Ma, SOT23-3	FMMT458TA	Diodes, Inc.
21	2	Q2 Q3	600 V, 0.4 A, 8 Ω , N-Channel, TO-92	STQ2NK60ZR-AP	ST Micro
22	1	R1	1 k Ω , 5%, 2 W, Metal Film	FMP200JR-52-1K	Yageo
23	2	R2 R8	130 Ω , 5%, 1 W, Thick Film, 2512	ERJ-1TYJ131U	Panasonic
24	2	R3 R4	162 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1623V	Panasonic
25	1	R5	30.1 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3012V	Panasonic
26	2	R6 R7	2 M Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2004V	Panasonic
27	1	R9	301 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3013V	Panasonic
28	2	R10 R11	10 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
29	1	R12	510 k Ω , 5%, 1/10 W, Thick Film, 1206	ERJ-8GEYJ514V	Panasonic
30	2	R13 R14	2.00 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
31	1	R15	200 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
32	1	R16	100 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ101V	Panasonic
33	1	R17	24.9 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2492V	Panasonic
34	1	R18	191 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1913V	Panasonic
35	1	R19	6.2 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ622V	Panasonic
36	1	R20	51 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ510V	Panasonic
37	1	R21	20 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ203V	Panasonic
38	2	R22 R23	1 M Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
39	2	R24 R25	24.9 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2492V	Panasonic
40	1	RV1	250 V, 21 J, 7 mm, RADIAL LA	V250LA4P	Littlefuse
41	1	T1	Custom	TSD-3192	Premier Magnetics
42	1	U1	LYTSwitch, eSIP-7C	LYT4311E	Power Integrations
43	1	VR1	15 V, 5%, 150 mW, SSMINI-2	DZ2S15000L	Panasonic-SSG
44	1	VR2	20 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5250B-7	Diodes, Inc.



7 Inductor Specification

7.1 Electrical Diagram

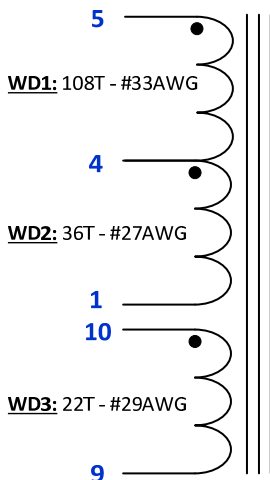


Figure 7 – Inductor Electrical Diagram.

7.2 Electrical Specifications

Primary Inductance	Pins 1-5, all other windings open, measured at 100 kHz, 0.4 RMS.	2 mH ±3%
Resonant Frequency	Pins 1-5, all other windings open.	800 kHz (Min.)

7.3 Materials

Item	Description
[1]	Core: EE13, NC2H.
[2]	Bobbin: EE13-Vertical, 10pins (5/5). Yih-Hwa Enterprises P/N: YW-538-02B.
[3]	Magnet wire: #33 AWG - Double coated.
[4]	Magnet wire: #27 AWG - Double coated.
[5]	Magnet wire: #29 AWG - Double coated.
[6]	Tape: 3M 1298 Polyester Film, 7.5 mm wide, 2.0 mils thick, or equivalent.
[7]	Varnish: Dolph BC-359 or equivalent.



7.4 Inductor Build Diagram

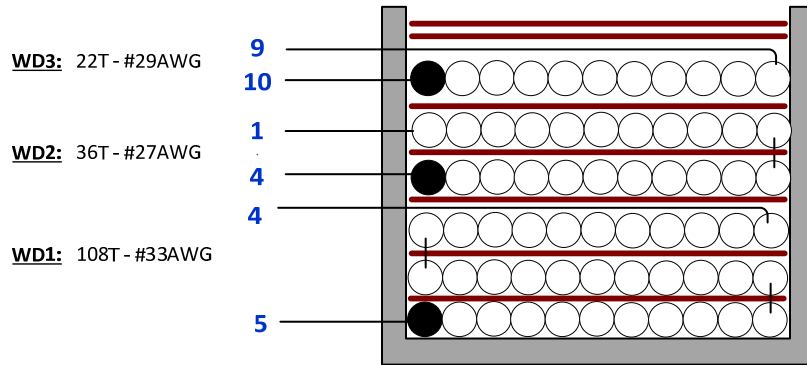


Figure 8 – Inductor Build Diagram.

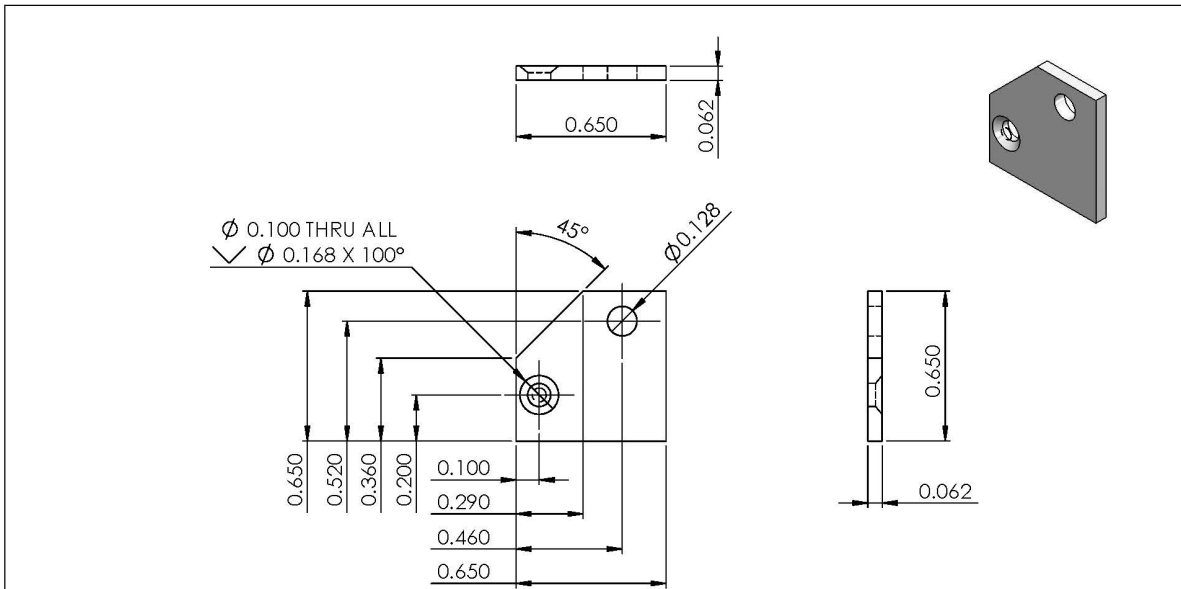
7.5 Inductor Construction

Winding Preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
WD1	Start at pin 5, wind 36 turns of wire item [3] from left to right, place 1 layer tape item [6], then continue wind another 36 turns from right to left, place 1 layer tape item [6], then continue wind another 36 turns from left to right, and end at pin 4.
Insulation	Place 1 layer of tape item [6].
WD2	Start at pin 4, wind 18 turns of wire item [4] from left to right, place 1 layer tape item [6], then continue wind another 18 turns from right to left, and end at pin 1.
Insulation	Place 1 layer of tape item [6].
WD3	Start at pin 10, wind 22 turns of wire item [5] from left to right in 1 layer. At the last turn bring the wire back to the left and end at pin 9.
Insulation	Place 2 layers of tape item [6].
Final Assembly	Grind, assemble, and secure core halves with tape. Varnish with item [7].




8 U1 Heat Sink

8.1 U1 Heat Sink Fabrication Drawing



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 Reports\DER-365 14.35W 41V 350mA HLO
 Dim Par20\Heatsink\PDF

 <p>POWER INTEGRATIONS</p> <p>The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com</p> <p>Copyright 2013, Power Integrations Proprietary and Confidential</p>	REMOVE ALL BURRS	UNLESS OTHERWISE SPECIFIED:	NAME	DATE	<p>Power Integrations</p> <p>TITLE: HEATSINK, DWG, DER365, PICUSTOM</p> <p>SIZE DWG. NO. REV A 61-00119-00 01</p> <p>SCALE: 5:1 WEIGHT: SHEET 1 OF 1</p>
	BREAK SHARP EDGES	DIMENSIONS ARE IN INCHES TOLERANCES: ANGULAR: MACH ± 0°30'	DRAWN BY: JNG	011613	
	PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS	XX ±0.1 XX ±0.01 XXX ±0.005	CHECKED BY:		
		ASME Y14.5	ENG APPR.		
	NEXT ASSY	MATERIAL AL-3003	MFG APPR.		
	USED ON	FINISH	Q.A.		
APPLICATION	DO NOT SCALE DRAWING	COMMENTS:			

5 4 3 2 1



8.2 U1 Heat Sink Assembly Drawing

1 FOR COMPLETED ASSEMBLY
SEE 61-00119-02.

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ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-001197-00	HEATSINK,AL,3003,DER365,PI CUSTOM	1
2	60-00051-00	POST,HEATSINK,SS,NICKEL PLATED,5mm W x 9.1 mm T	1
3	75-00084-00	RIVET,Al,,093 DIA x 0.187 C'sunk	1

POWER INTEGRATIONS

The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com

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REMOVE ALL BURRS	UNLESS OTHERWISE SPECIFIED:	NAME	DATE	Power Integrations TITLE: HEATSINK, DWG, DER365, PI CUSTOM SIZE A DWG. NO. 61-00119-01 REV 01 SCALE: 2:1 WEIGHT: SHEET 1 OF 1
BREAK SHARP EDGES	DIMENSIONS ARE IN INCHES	DRAWN BY: JNG	013013	
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS	TOLERANCES: ANGULAR: MACH ± 0°30' X.X ±0.1 X.XX ±0.01 X.XXX ±0.005	CHECKED BY:		
	ASME Y14.5	ENG APPR.		
NEXT ASSY	MATERIAL	MFG APPR.		
USED ON	FINISH	Q.A.		
APPLICATION	DO NOT SCALE DRAWING	COMMENTS:		

8.3 Heat Sink and U1 Assembly Drawing

ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00119-00	HEATSINK, CUSTOM, DER365	1
2	75-00001-00	SCREW MACHINE PHIL 4-40 X 1/4 SS	1
3	75-00164-00	WASHER FLAT #4 ZINC, OD 0.219 ID 0.125, THK 0.032, YELLOW CHROME FINISH	1
4	60-00037-00	HEATSINK HARDWARE, EDGE CLIP, 12.40mmL x 6.50mmW	1
5	75-00068-00	NUT, HEX, KEP4-40, ZINC PLATE	1
6	10-00638-00	LYTswitch, LYT4311E, eSIP-7C	1
7	60-00035-00	THERMAL GREASE, SILICONE, 5 OZ TUBE	1

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REMOVE ALL BURRS	UNLESS OTHERWISE SPECIFIED:	NAME	DATE	Power Integrations TITLE: HEATSINK, ASSY, ESIP, DER365, PI CUSTOM SIZE DWG. NO. REV A 61-00119-02 01 SCALE: 1:1 WEIGHT: SHEET 1 OF 1
BREAK SHARP EDGES	DIMENSIONS ARE IN INCHES	DRAWN BY:	JNG 022713	
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS	TOLERANCES: ANGULAR: MACH ± 0°30' X.X ±0.1 X.XX ±0.01 X.XXX ±0.005	CHECKED BY:		
	ASME Y14.5	ENG APPR.		
NEXT ASSY	MATERIAL	MFG APPR.		
USED ON	FINISH	Q.A.		
APPLICATION	DO NOT SCALE DRAWING	COMMENTS:		

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9 Performance Data

All measurements performed at room temperature using an LED load. The following data was taken measured using 3 sets of loads representing a load range of 38 V to 44 V (output voltage). Refer to the table on Section 9.6 for complete test data values.

9.1 Efficiency

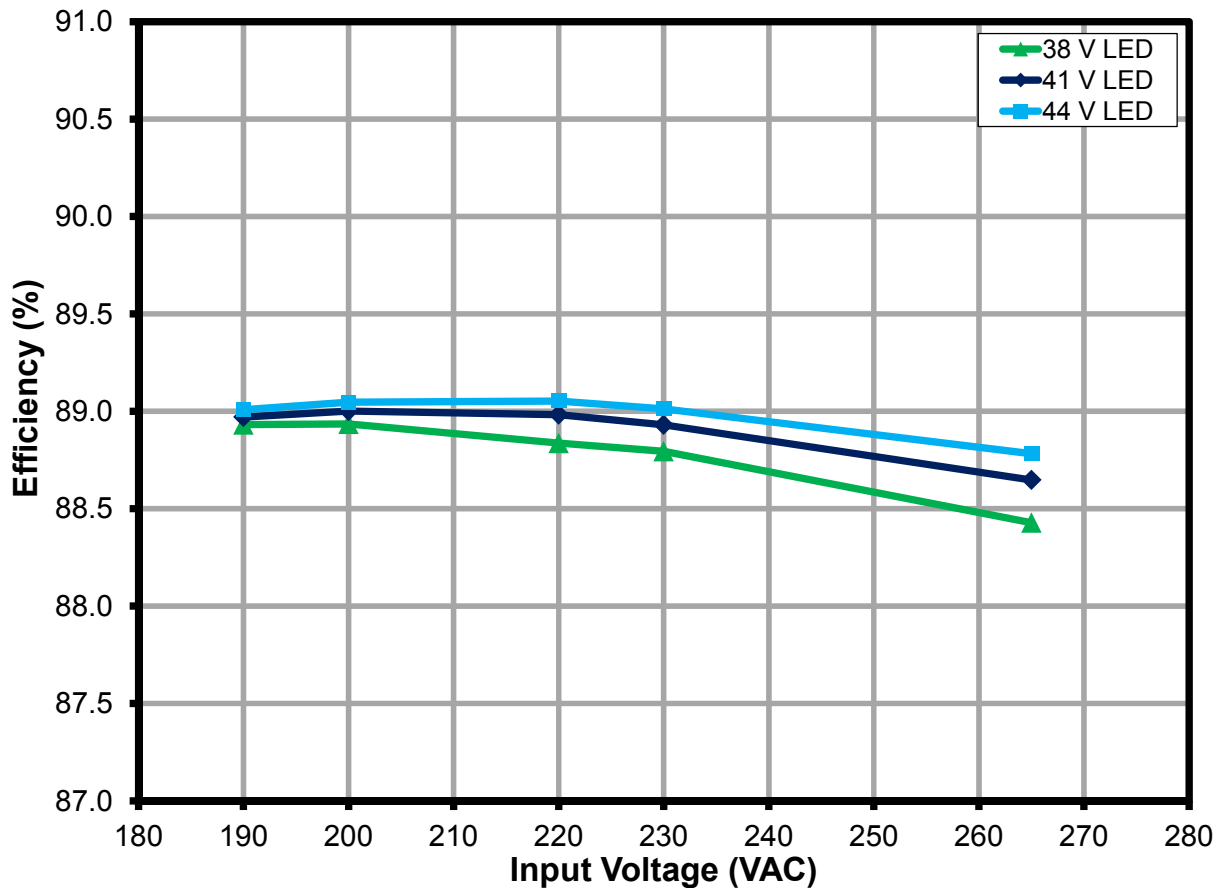


Figure 9 – Efficiency vs. Line and Load.



9.2 Line and Load Regulation

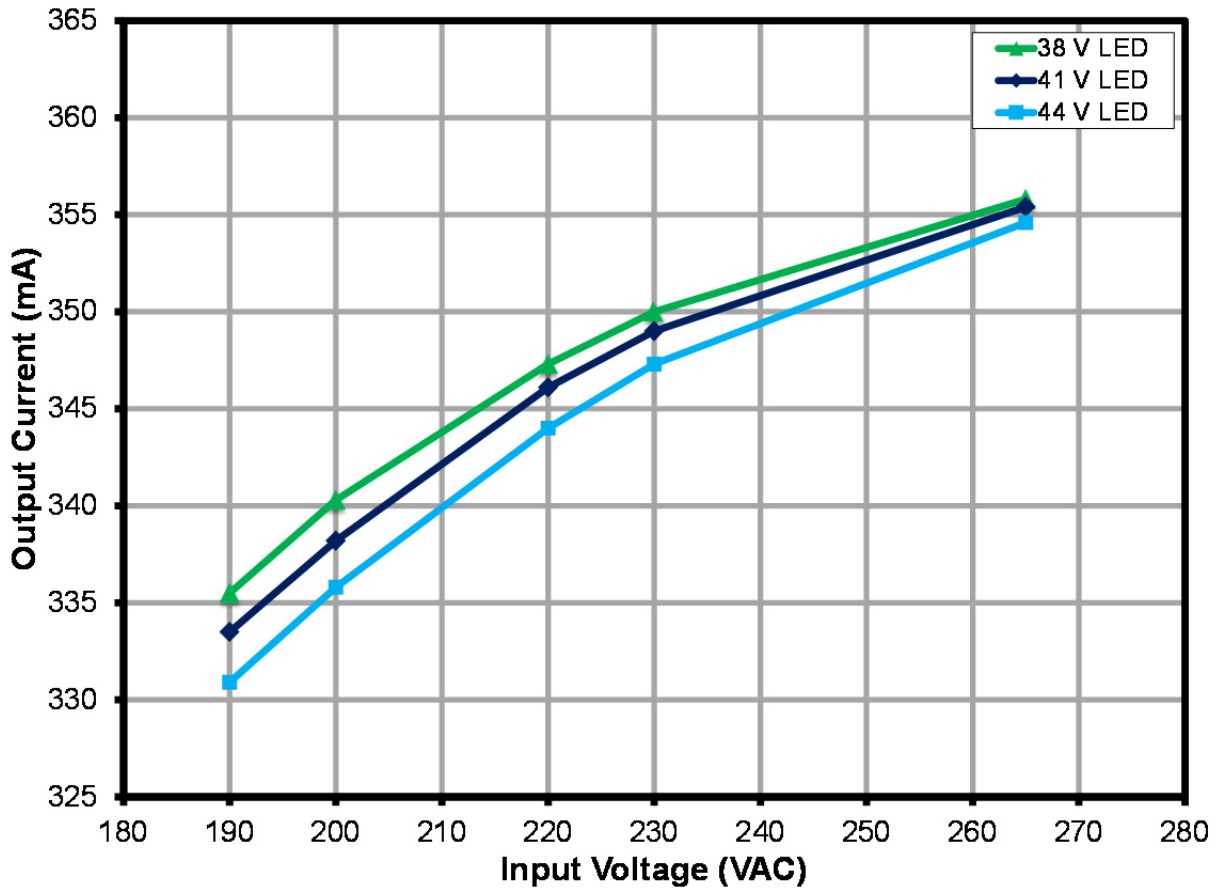


Figure 10 – Regulation vs. Line and Load.



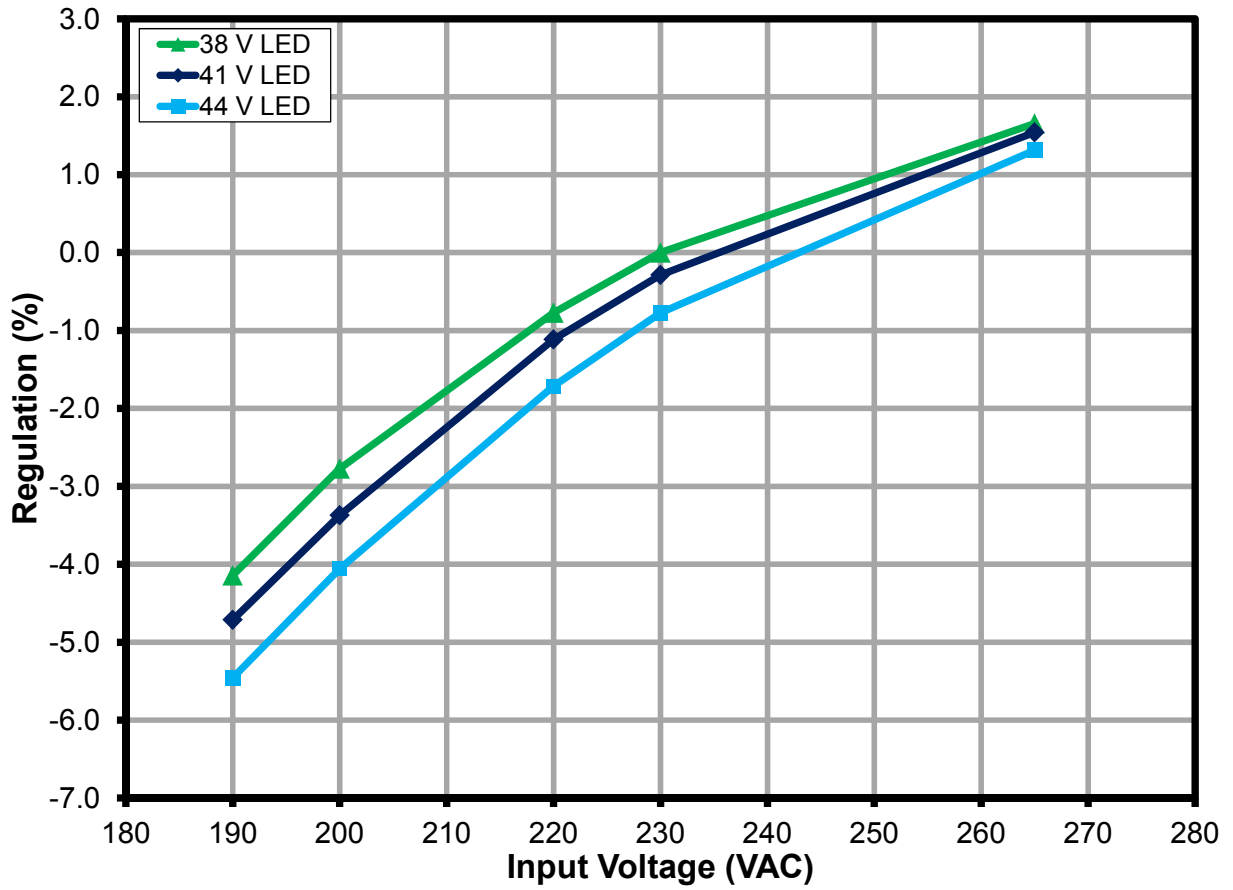


Figure 11 – % Regulation vs. Line and Load.



9.3 Power Factor

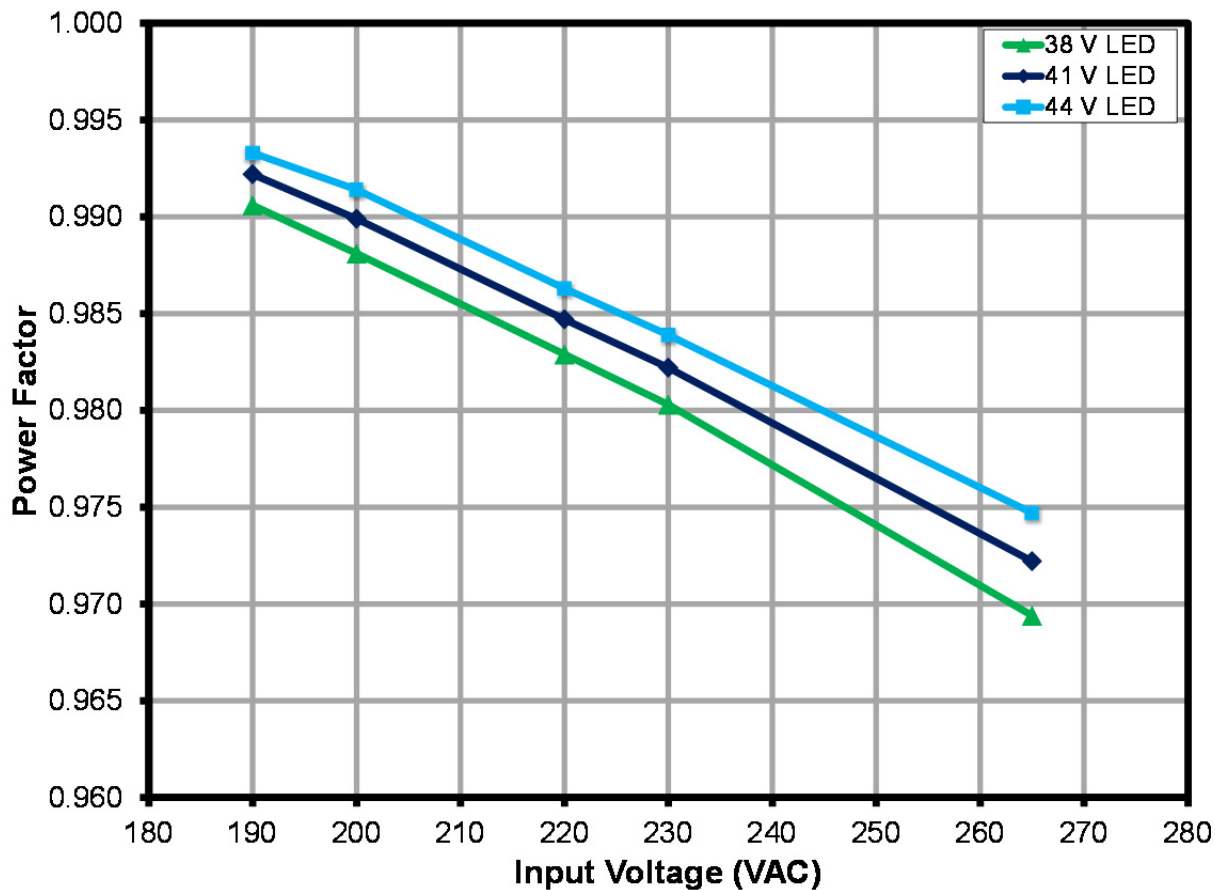


Figure 12 – Power Factor vs. Line and Load.



9.4 A-THD

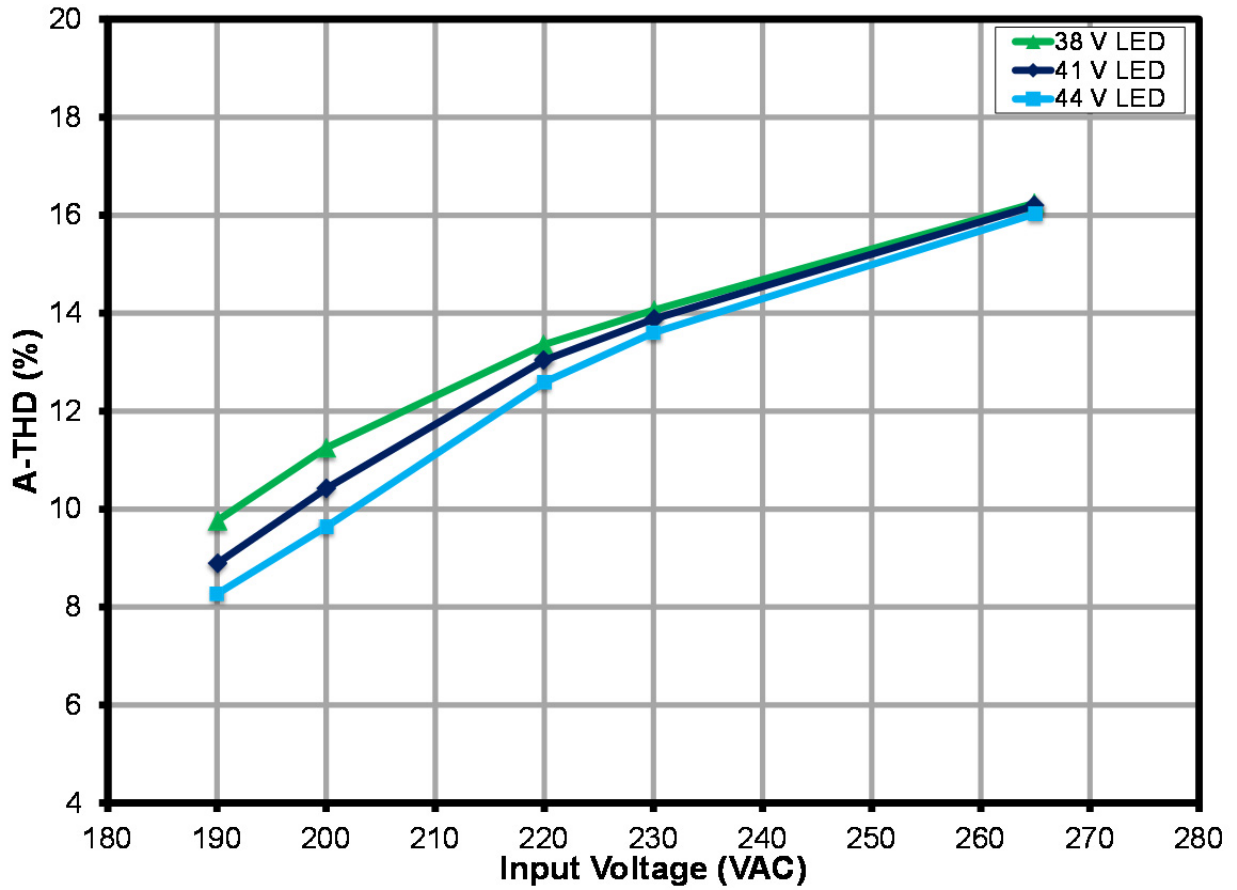


Figure 13 – A-THD vs. Line and Load.



9.5 Harmonics

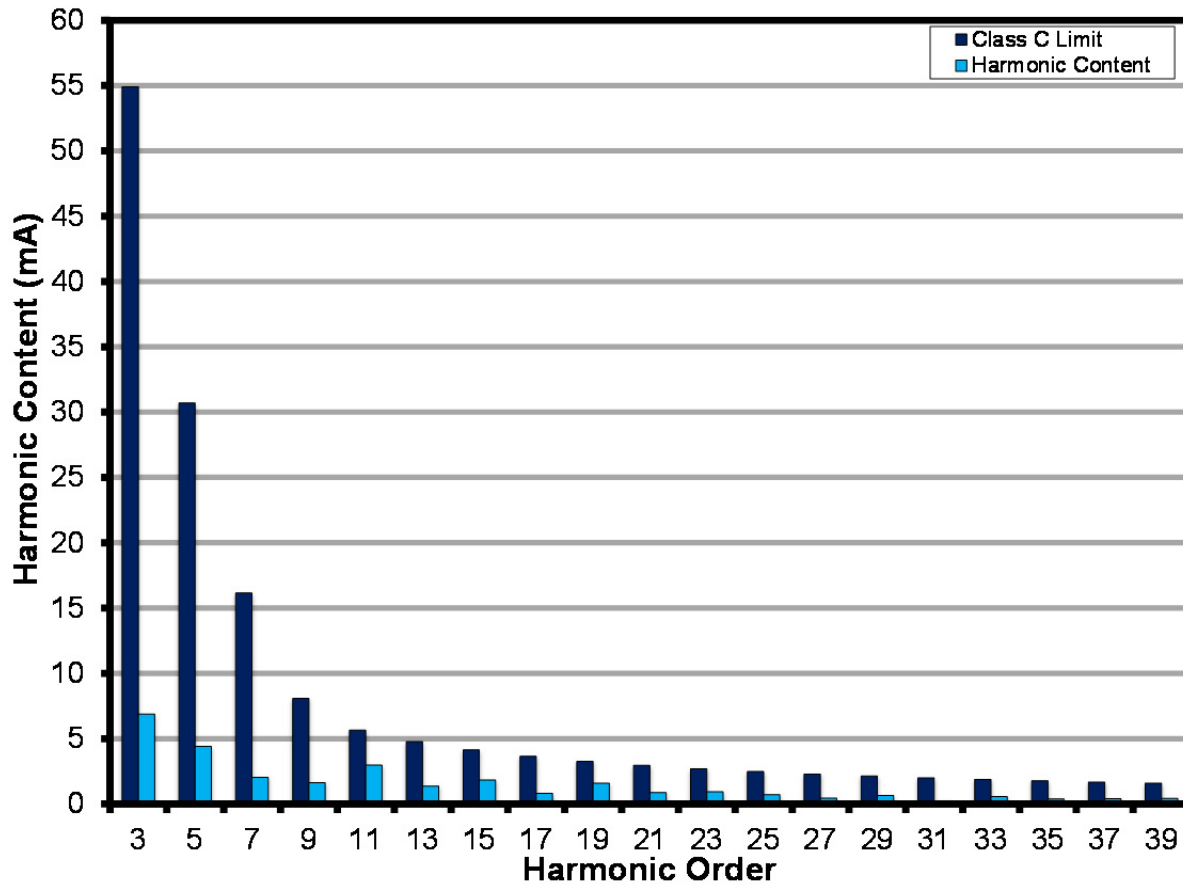


Figure 14 – 41 V LED Load Input Current Harmonics at 230 VAC, 50 Hz.



9.6 Test Data

All measurements were taken with the board at open frame, 25 °C ambient, and 50 Hz line frequency.

9.6.1 Test Data, 38 V LED Load

Input		Input Measurement					Load Measurement				
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	Efficiency (%)	% Reg
190	50	190.33	76.15	14.357	0.991	9.76	37.9830	335.500	12.768	88.93	-4.14
200	50	200.34	73.59	14.569	0.988	11.25	38.0080	340.300	12.957	88.94	-2.77
220	50	220.38	68.78	14.898	0.983	13.36	38.0430	347.300	13.235	88.84	-0.77
230	50	230.37	66.55	15.029	0.980	14.06	38.0620	350.000	13.345	88.79	0.00
265	50	265.48	59.64	15.348	0.969	16.25	38.0850	355.800	13.572	88.43	1.66

9.6.2 Test Data, 41 V LED Load

Input		Input Measurement					Load Measurement				
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	Efficiency (%)	% Reg
190	50	190.31	81.53	15.395	0.992	8.89	41.0100	333.500	13.697	88.97	-4.71
200	50	200.33	78.77	15.621	0.990	10.42	41.0400	338.200	13.903	89.00	-3.37
220	50	220.35	73.75	16.003	0.985	13.04	41.0850	346.100	14.240	88.98	-1.11
230	50	230.41	71.37	16.152	0.982	13.88	41.0990	349.000	14.364	88.93	-0.29
265	50	265.48	64.00	16.517	0.972	16.2	41.1390	355.400	14.642	88.65	1.54

9.6.3 Test Data, 44 V LED Load

Input		Input Measurement					Load Measurement				
VAC (V _{RMS})	Freq (Hz)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	PF	%ATHD	V _{OUT} (V _{DC})	I _{OUT} (mA _{DC})	P _{OUT} (W)	Efficiency (%)	% Reg
190	50	190.33	86.67	16.385	0.993	8.27	44.0050	330.900	14.584	89.01	-5.46
200	50	200.33	83.71	16.625	0.991	9.64	44.0310	335.800	14.804	89.05	-4.06
220	50	220.39	78.45	17.054	0.986	12.59	44.0860	344.000	15.187	89.05	-1.71
230	50	230.41	76.01	17.230	0.984	13.6	44.1070	347.300	15.337	89.01	-0.77
265	50	265.47	68.25	17.660	0.975	16.03	44.1540	354.600	15.679	88.78	1.31



10 Dimming Performance Data

TRIAC dimming results were taken with input voltage of 230 VAC, 50 Hz line frequency, room temperature, and nominal 41 V LED load.

10.1 Dimming Curve with Leading Edge Type Dimmer

Taken using programmable AC source providing leading edge chopped AC input.

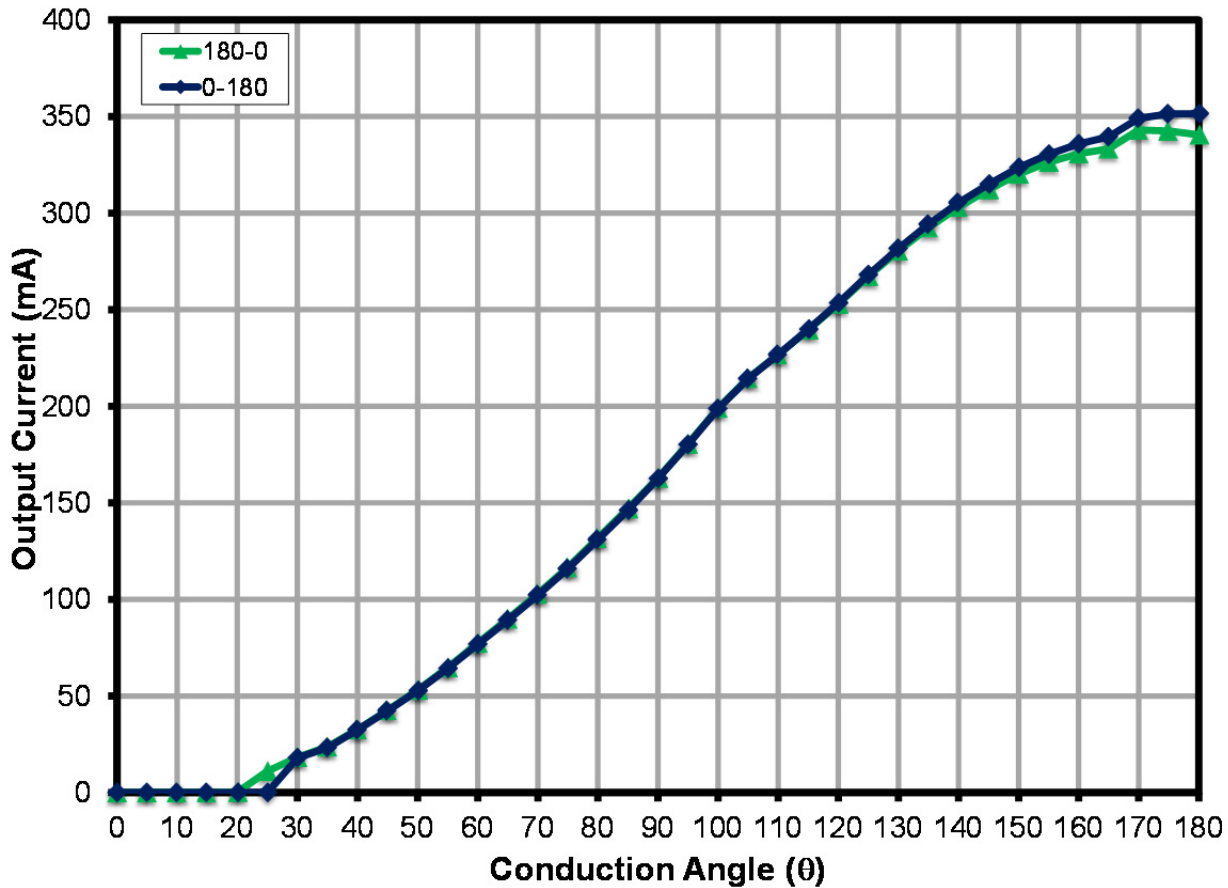


Figure 15 – Leading Edge Dimming Characteristics.



10.2 Dimmer Compatibility List

The unit was tested with the following high-line dimmers at 230 VAC, 50 Hz input and 41 V LED load and using Agilent 6812B AC source.

Chinese Dimmers	Type	Maximum Setting I _{OUT} (mA)	Minimum Setting I _{OUT} (mA)	Dim Ratio
TCL 630 W	L	334	15	22
EBA HUANG	L	337	1	337
SB ELECT 600 W	L	326	2	163
MYONGBO	L	336	40	8
CLIPMEI	L	333	3	111
MANK 200 W	L	334	54	6

German Dimmers	Type	Maximum Setting I _{OUT} (mA)	Minimum Setting I _{OUT} (mA)	Dim Ratio
REV 300 W	L	317	1	317
BUSCH 2250	L	320	25	13
MERTEN 572499	L	331	15	22
BERKER 2875 600 W	L	317	30	11
KOPP 8033	L	293	25.9	11

Korean Dimmers	Type	Maximum Setting I _{OUT} (mA)	Minimum Setting I _{OUT} (mA)	Dim Ratio
ANAM 500W	L	332	90	4
SHIN SUNG 500W	L	336	66	5
FANTASIA 500W	L	337	44	8

EU Dimmers	Type	Maximum Setting I _{OUT} (mA)	Minimum Setting I _{OUT} (mA)	Dim Ratio
BERKER 2830 10	L	317	37	9
JUNG 225 NV DE	L	310	24.6	13
JUNG 266 G DE	L	318	32	10
BUSCH 2200 UJ-212	L	317	44	7
BUSCH 2250 U	L	326	4.3	76
BUSCH 2247 U	L	317	43.7	7
GIRA 2262 00 / IO1	L	318	16	20
GIRA 0300 00 / IO1	L	315	43	7
GIRA 0302 00 / IO1	L	318	33	10

Trailing Edge Dimmers	Type	Maximum Setting I _{OUT} (mA)	Minimum Setting I _{OUT} (mA)	Dim Ratio
PEHA 433HAB	T	311	78	4
PEHA 433HAB oA	T	274	48	6
BUSCH 6513	T	341	89	4
JUNG 254 UDIE 1	T	315	97	3

Figure 16 – Compatibility List.



11 Thermal Performance

Images captured after running for >30 minutes at room temperature (25 °C), open frame for the conditions specified.

NOTE: Potting the board or placing heat sink on U1 may be necessary when used at high ambient conditions.

11.1 Non-Dimming $V_{IN} = 190 \text{ VAC}, 50 \text{ Hz}, 41 \text{ V LED Load}$

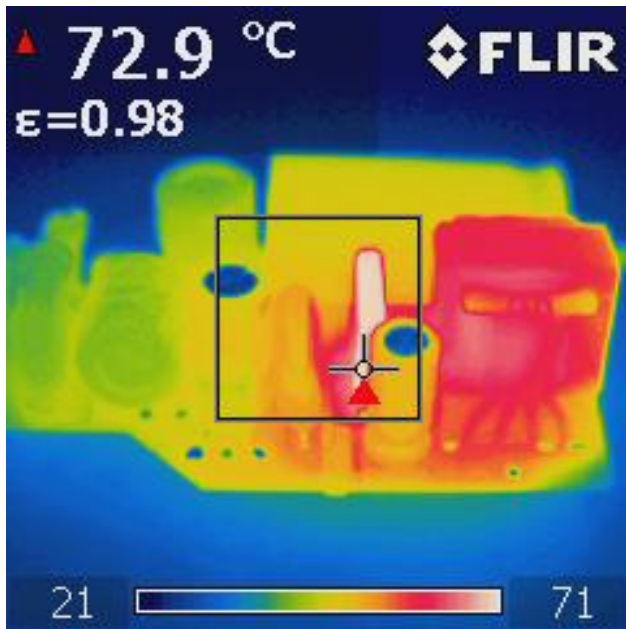


Figure 17 – Top Side.
U1-LYT4311E: 72.9 °C.

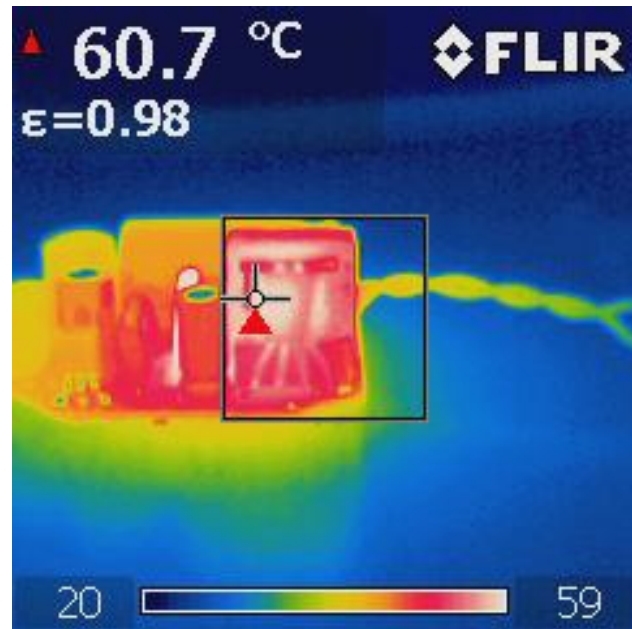


Figure 18 – Top Side.
T1: 60.7 °C.

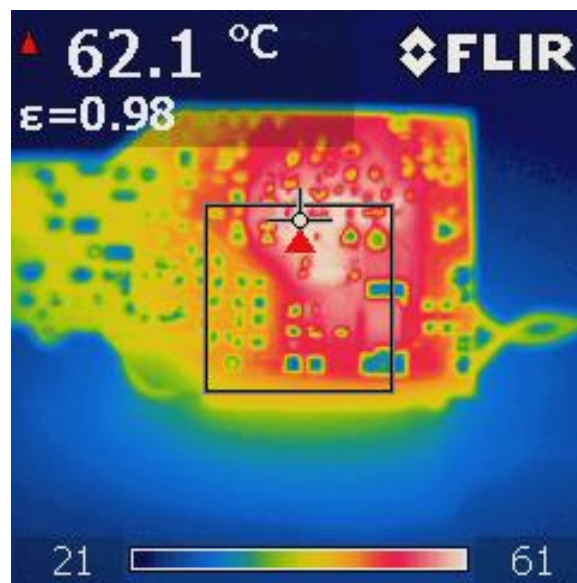


Figure 19 – Bottom Side.
PCB: 62.1 °C.

11.2 Non-Dimming $V_{IN} = 265 \text{ VAC}$, 50 Hz, 41 V LED Load

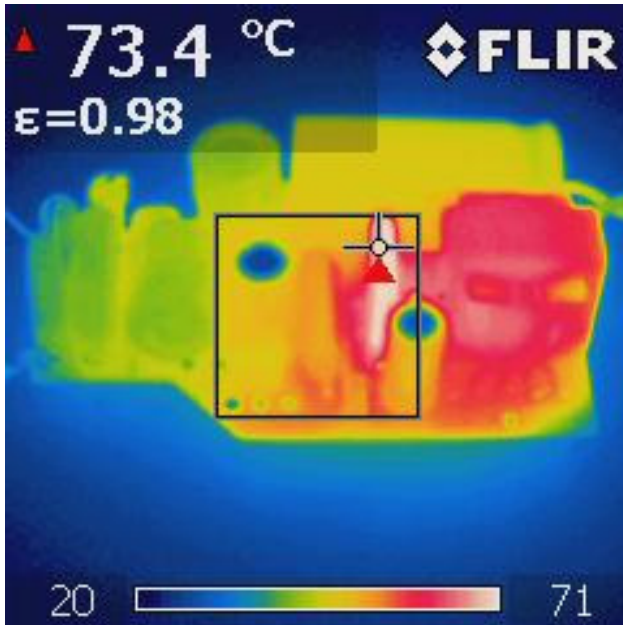


Figure 20 – Top Side.
U1-LYT4311E: 73.4 °C.

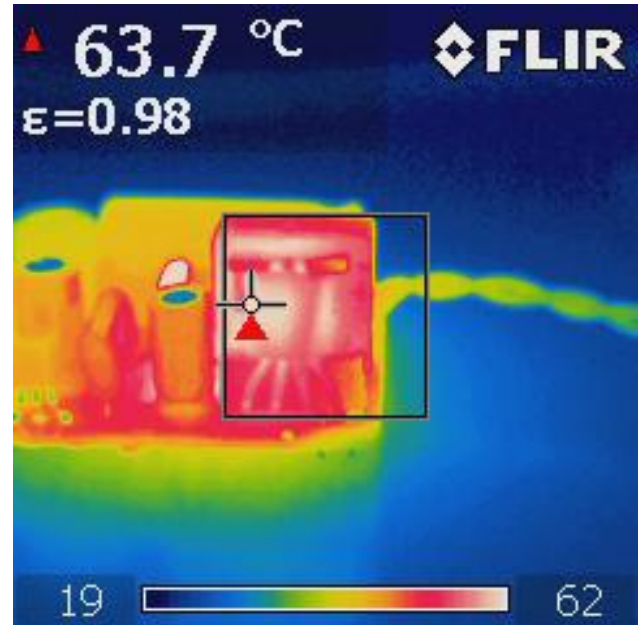


Figure 21 – Top Side, Inductor.
T1: 63.7 °C.

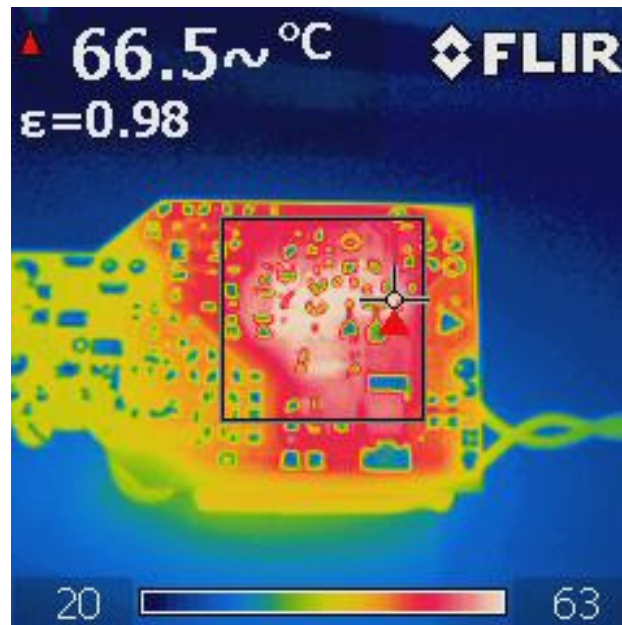


Figure 22 – Bottom Side.
PCB: 66.5 °C.

11.3 Dimming $V_{IN} = 230 \text{ VAC}$, 50 Hz, 41 V LED Load, REV300 Dimmer

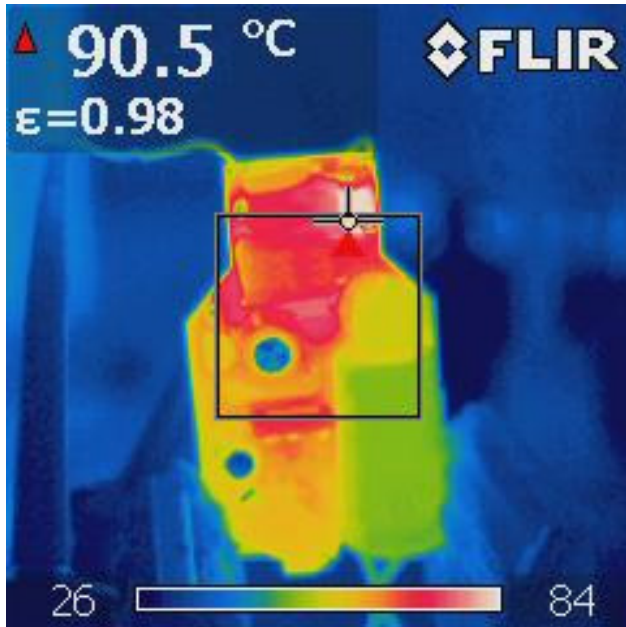


Figure 23 – 90° Conduction Angle.
R26: 90.5 °C.

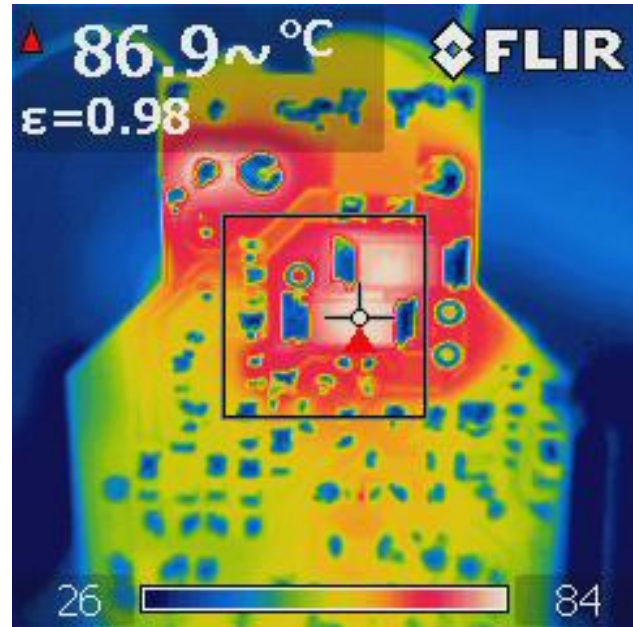


Figure 24 – 90° Conduction Angle.
R2: 86.9 °C.

12 Non-Dimming Waveforms

12.1 Input Voltage and Input Current Waveforms

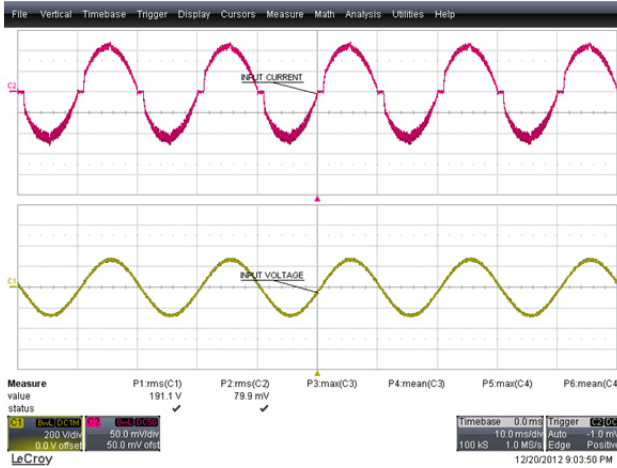


Figure 25 – 190 VAC, Full Load.
 Upper: I_{IN} , 50 mA / div.
 Lower: V_{IN} , 200 V, 10 ms / div.

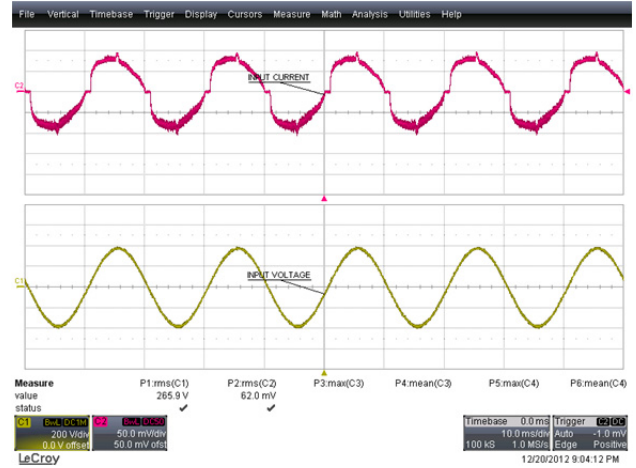


Figure 26 – 265 VAC, Full Load.
 Upper: I_{IN} , 50 mA / div.
 Lower: V_{IN} , 200 V, 10 ms / div.

12.2 Output Current and Output Voltage at Normal Operation

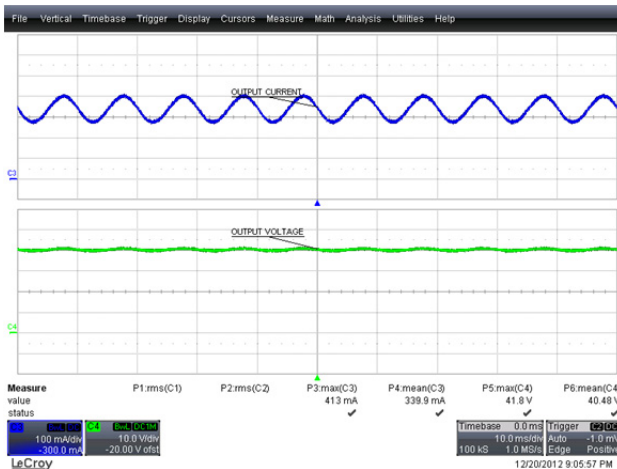


Figure 27 – 190 VAC, 50 Hz Full Load.
 Upper: I_{OUT} , 100 mA / div.
 Lower: V_{OUT} , 10 V, 10 ms / div.

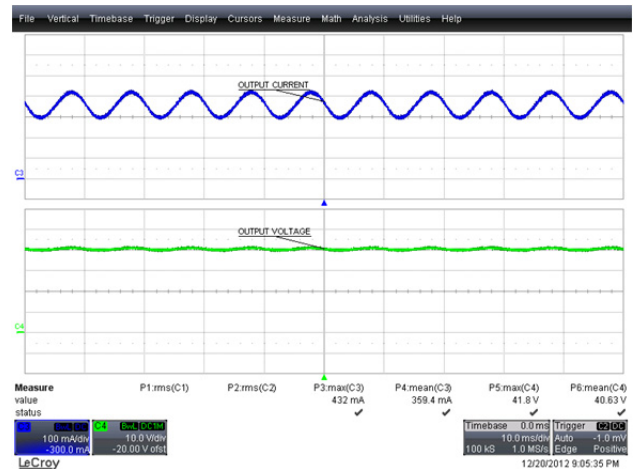


Figure 28 – 265 VAC, 50 Hz Full Load.
 Upper: I_{OUT} , 100 mA / div.
 Lower: V_{OUT} , 10 V, 10 ms / div.



12.3 Input Voltage and Output Current Waveform at Start-up

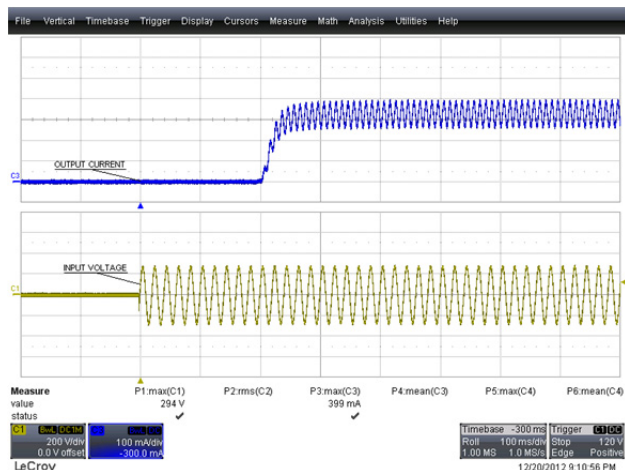


Figure 29 – 190 VAC, 50 Hz.
Upper: I_{OUT} , 100 mA / div.
Lower: V_{IN} , 200 V, 100 ms / div.

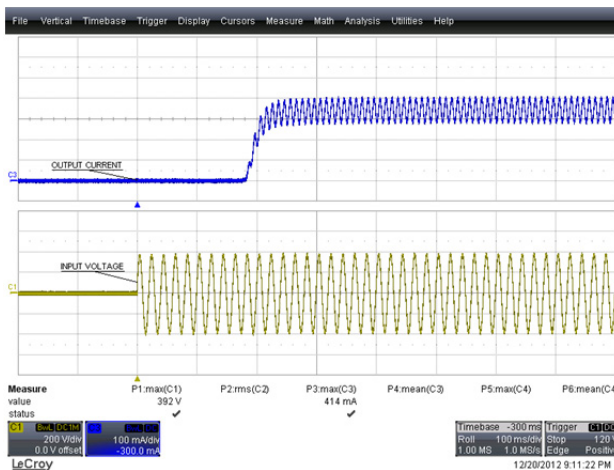


Figure 30 – 265 VAC, 50 Hz.
Upper: I_{OUT} , 100 mA / div.
Lower: V_{IN} , 200 V, 100 ms / div.

12.4 Drain Voltage and Current at Normal Operation

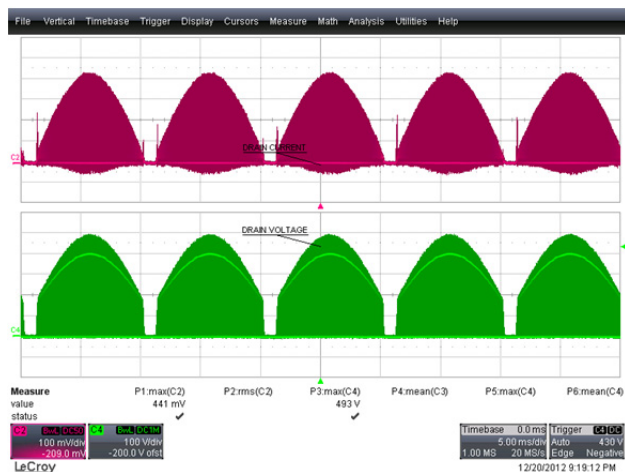


Figure 31 – 190 VAC, 50 Hz.
Upper: I_{DRAIN} , 100 mA / div.
Lower: V_{DRAIN} , 100 V, 5 ms / div.

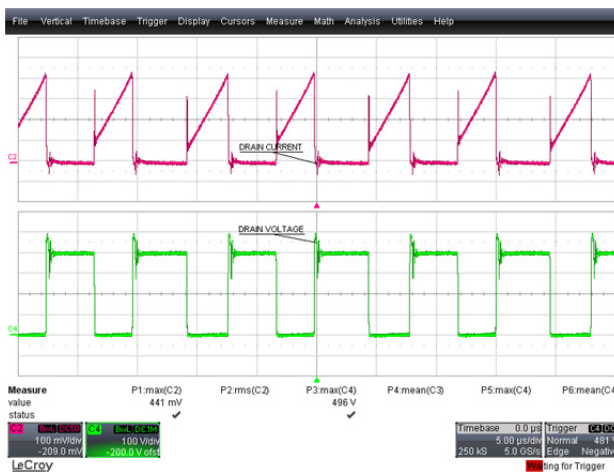


Figure 32 – 190 VAC, 50 Hz.
Upper: I_{DRAIN} , 100 mA / div.
Lower: V_{DRAIN} , 100 V / div., 5 μ s / div.



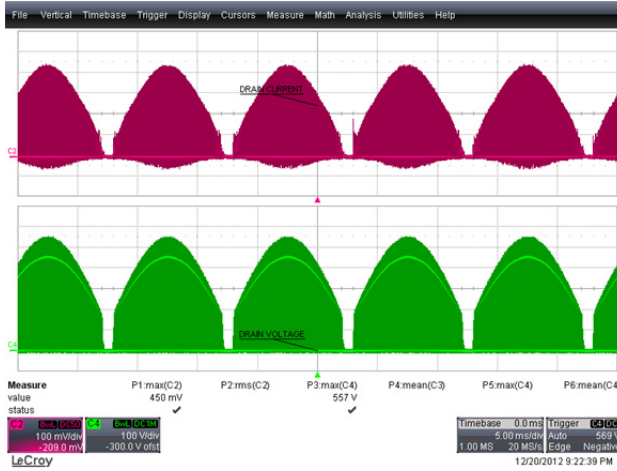


Figure 33 – 230 VAC, 50 Hz.
 Upper: I_{DRAIN} , 100 mA / div.
 Lower: V_{DRAIN} , 100 V, 5 ms / div.

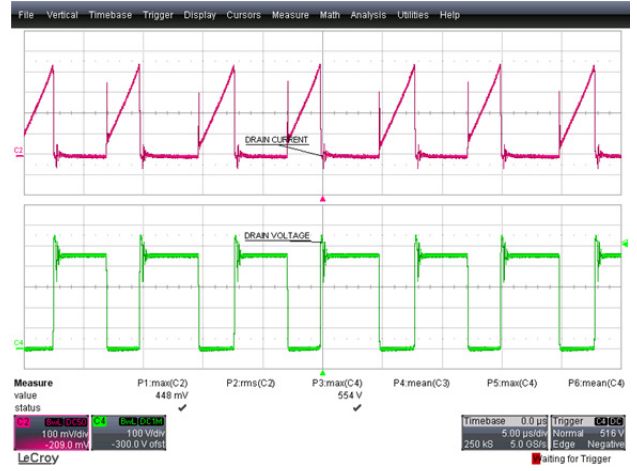


Figure 34 – 230 VAC, 50 Hz.
 Upper: I_{DRAIN} , 100 mA / div.
 Lower: V_{DRAIN} , 100 V / div., 5 μ s / div.

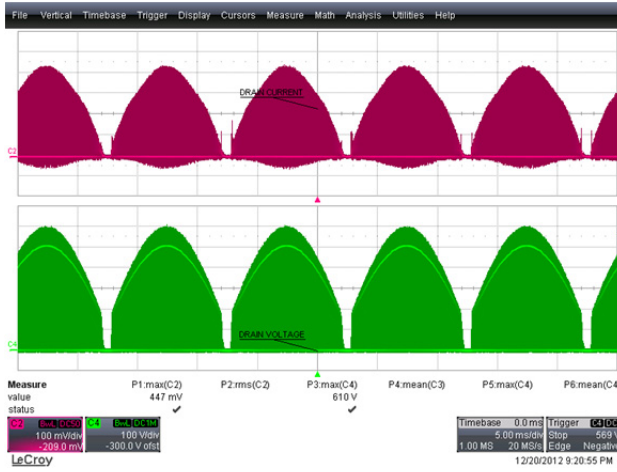


Figure 35 – 265 VAC, 50 Hz.
 Upper: I_{DRAIN} , 100 mA / div.
 Lower: V_{DRAIN} , 100 V, 5 ms / div.



Figure 36 – 265 VAC, 50 Hz.
 Upper: I_{DRAIN} , 100 mA / div.
 Lower: V_{DRAIN} , 100 V / div., 5 μ s / div.

12.5 Start-up Drain Voltage and Current

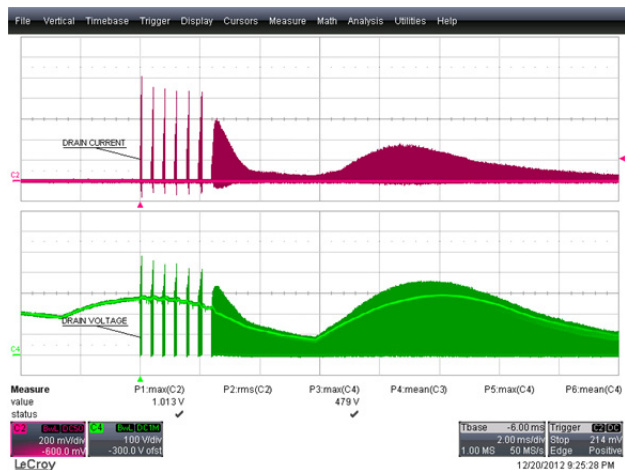


Figure 37 – 190 VAC, 50 Hz Start-up.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 100 V, 2 ms / div.



Figure 38 – 190 VAC, 50 Hz Start-up.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 100 V, 10 μ s / div.



Figure 39 – 265 VAC, 50 Hz Start-up.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 100 V, 2 ms / div.

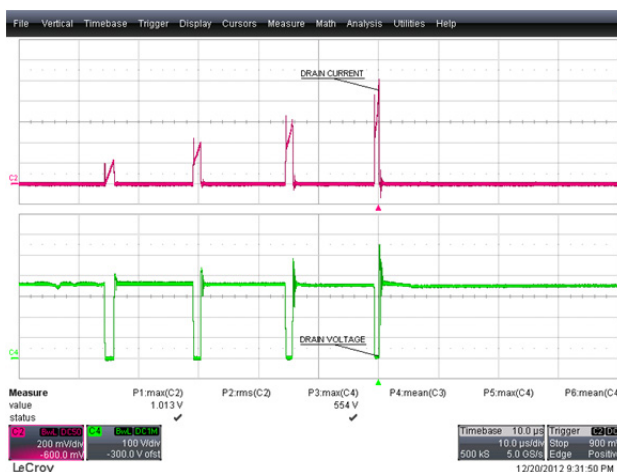


Figure 40 – 265 VAC, 50 Hz Start-up.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 100 V, 10 μ s / div.



12.6 Drain Current and Drain Voltage during Output Short Condition



Figure 41 – 190 VAC, 50 Hz Output Short Condition.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 100 V, 200 ms / div.



Figure 42 – 190 VAC, 50 Hz Output Short Condition.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 100 V, 10 μ s / div.

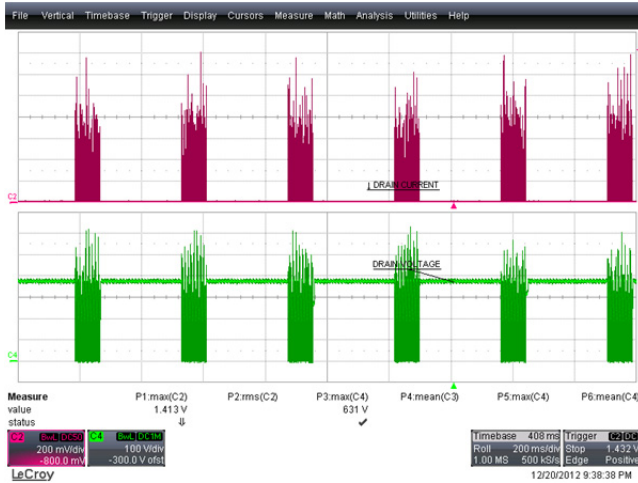


Figure 43 – 265 VAC, 50 Hz Output Short Condition.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 100 V, 200 ms / div.

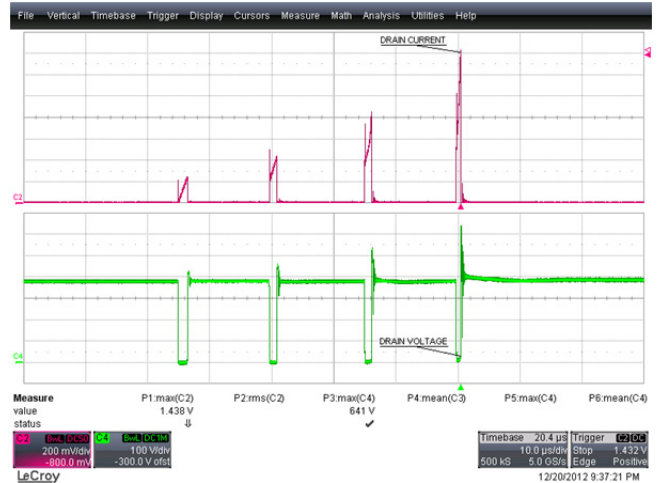


Figure 44 – 265 VAC, 50 Hz Output Short Condition.
 Upper: I_{DRAIN} , 200 mA / div.
 Lower: V_{DRAIN} , 100 V, 10 μ s / div.



12.7 Output Diode Current and Voltage Waveforms

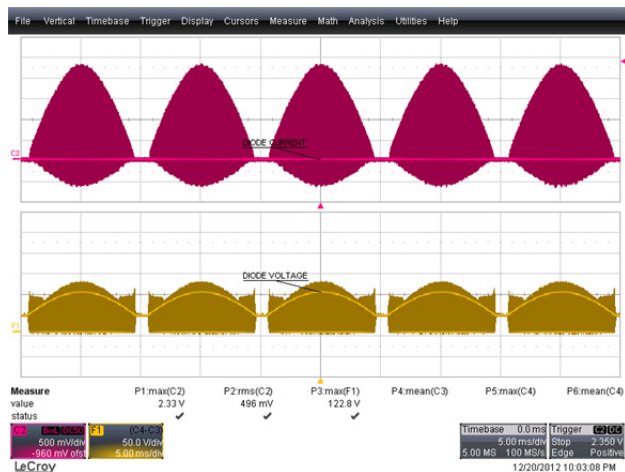


Figure 45 – 190 VAC, 50 Hz.
 Upper: I_{D7} , 0.5 A / div.
 Lower: V_{D7} , 50 V, 5 ms / div.

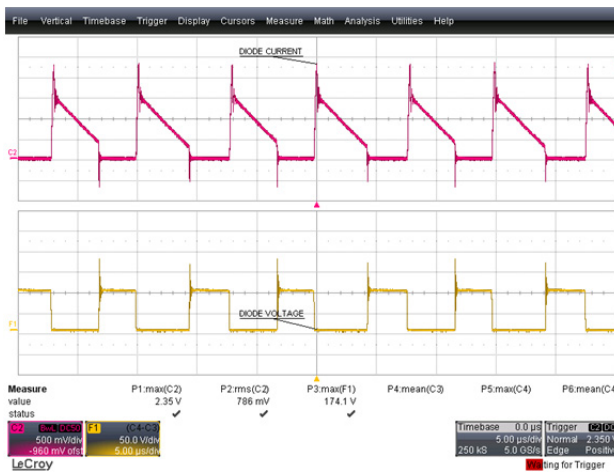


Figure 46 – 190 VAC, 50 Hz.
 Upper: I_{D7} , 0.5 A / div.
 Lower: V_{D7} , 50 V / div., 5 μ s / div.

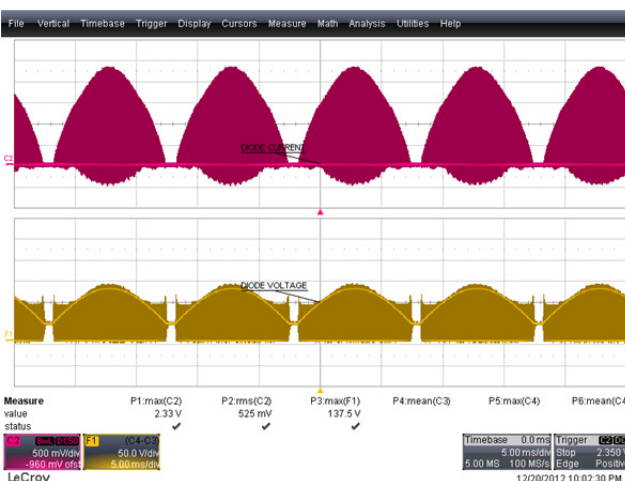


Figure 47 – 265 VAC, 50 Hz.
 Upper: I_{D7} , 0.5 A / div.
 Lower: V_{D7} , 50 V, 5 ms / div.

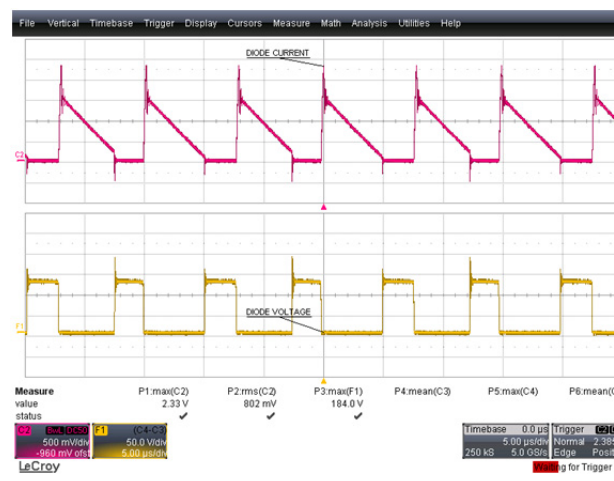


Figure 48 – 265 VAC, 50 Hz.
 Upper: I_{D7} , 0.5 A / div.
 Lower: V_{D7} , 50 V / div., 5 μ s / div.



12.8 Output Diode Current and Voltage Start-up Waveforms

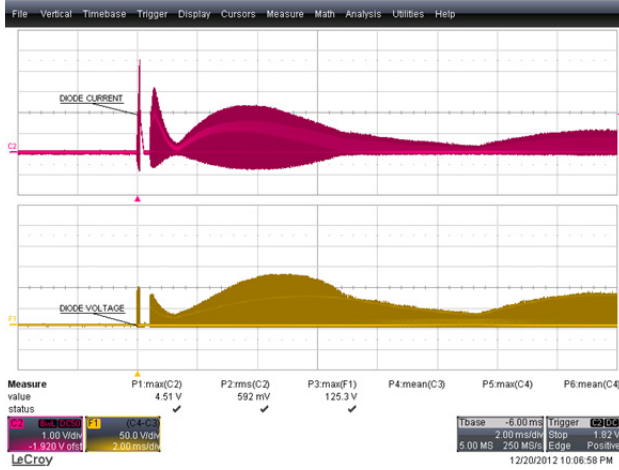


Figure 49 – 190 VAC, 50 Hz.
 Upper: I_{D7} , 1 A / div.
 Lower: V_{D7} , 50 V, 2 ms / div.

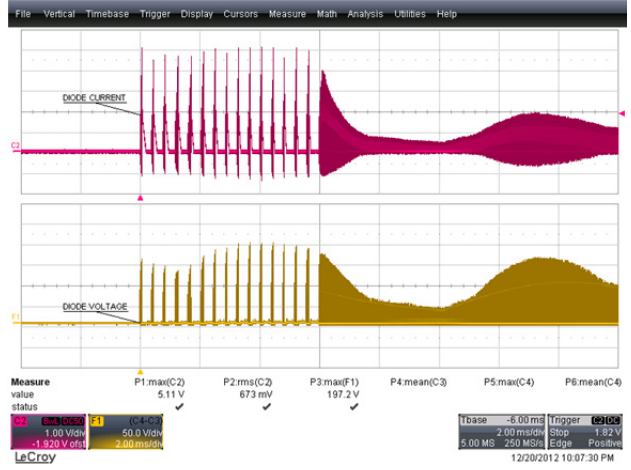


Figure 50 – 265 VAC, 50 Hz.
 Upper: I_{D7} , 1 A / div.
 Lower: V_{D7} , 50 V / div., 2 ms / div.

12.9 Output Diode Current and Voltage Short-Circuit Waveforms

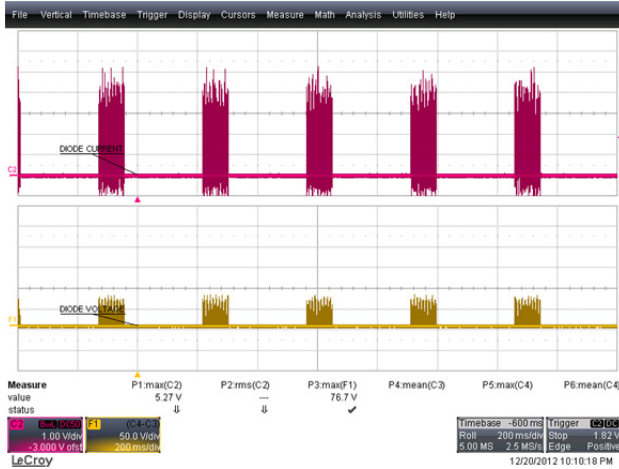


Figure 51 – 190 VAC, 50 Hz.
 Upper: I_{D7} , 1 A / div.
 Lower: V_{D7} , 50 V, 200 ms / div.

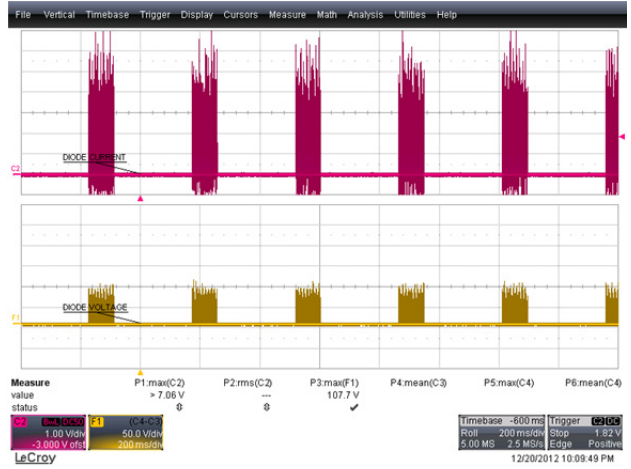


Figure 52 – 265 VAC, 50 Hz.
 Upper: I_{D7} , 1 A / div.
 Lower: V_{D7} , 50 V / div., 200 ms / div.



12.10 Brown-out

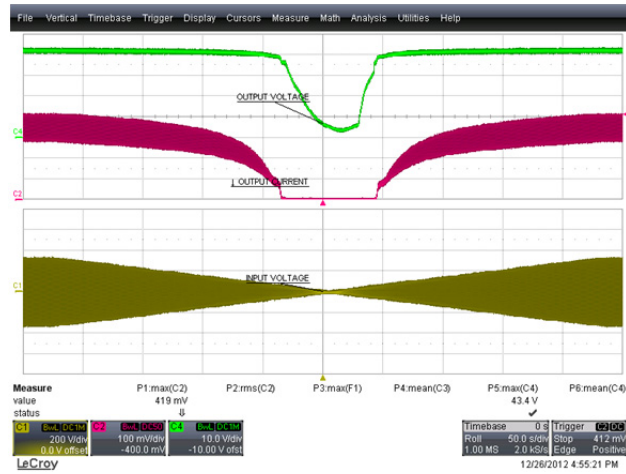


Figure 53 – 230 VAC, 50 Hz.
 CH4: V_{OUT} , 10 V / div.
 CH2: I_{OUT} , 100 mA / div.
 CH1: V_{IN} , 200 V / div.



12.11 Line Transient

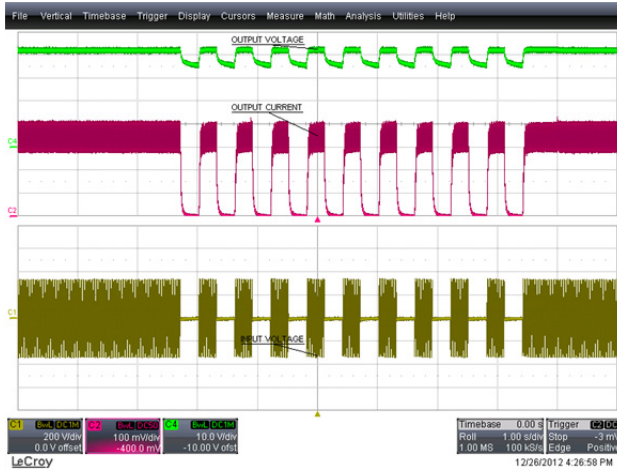


Figure 54 – 230 VAC, 50 Hz.
 300 ms ON, 300 ms OFF.
 CH4: V_{OUT}, 10 V / div.
 CH2: I_{OUT}, 100 mA / div.
 CH1: V_{IN}, 200 V / div.

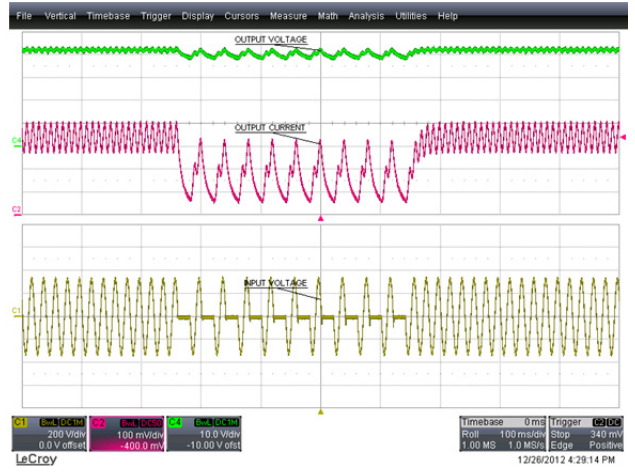


Figure 55 – 230 VAC, 50 Hz.
 20 ms ON, 20 ms OFF.
 CH4: V_{OUT}, 10 V / div.
 CH2: I_{OUT}, 100 mA / div.
 CH1: V_{IN}, 200 V / div.

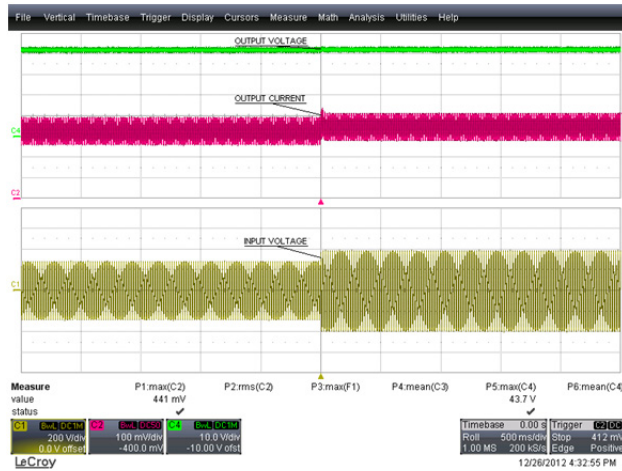


Figure 56 – 190 V to 265 V Step.
 CH4: V_{OUT}, 10 V / div.
 CH2: I_{OUT}, 100 mA / div.
 CH1: V_{IN}, 200 V / div.



13 Dimming Waveforms

13.1 Input Voltage and Input Current Waveforms

Input: 230 VAC, 50 Hz

Output: 41 V LED Load

Dimmer: MERTEN 572499 400 W

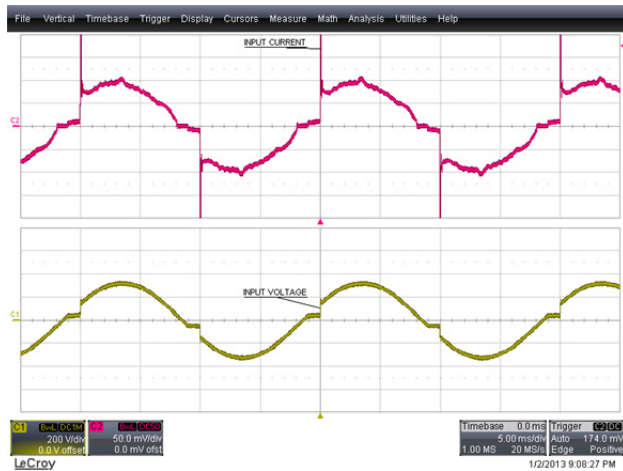


Figure 57 – 160° Conduction Angle.
Upper: I_{IN} , 50 mA / div.
Lower: V_{IN} , 200 V, 5 ms / div.

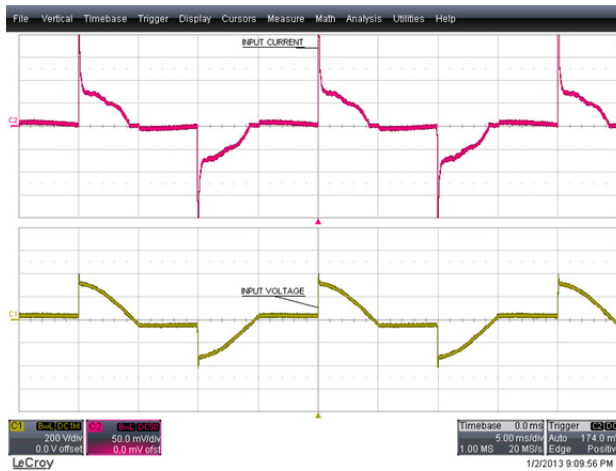


Figure 58 – 90° Conduction Angle.
Upper: I_{IN} , 50 mA / div.
Lower: V_{IN} , 200 V, 5 ms / div.



Figure 59 – 60° Conduction Angle.
Upper: I_{IN} , 50 mA / div.
Lower: V_{IN} , 200 V, 5 ms / div.



Figure 60 – 45° Conduction Angle.
Upper: I_{IN} , 50 mA / div.
Lower: V_{IN} , 200 V, 5 ms / div.



13.2 Output Current Waveforms

Input: 230 VAC, 50 Hz

Output: 41 V LED Load

Dimmer: MERTEN 572499 400 W

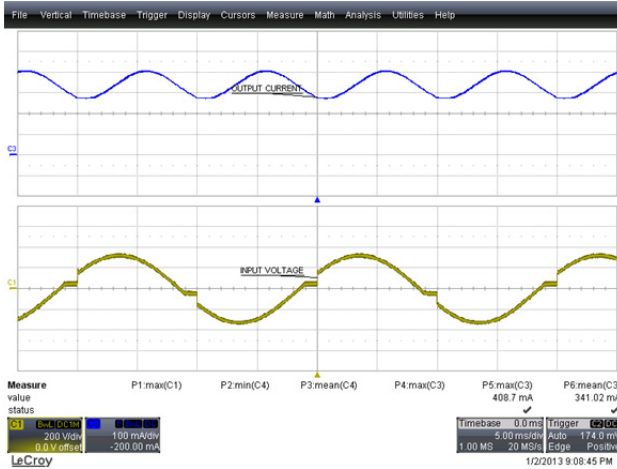


Figure 61 – 160° Conduction Angle.
 Upper: I_{OUT} , 100 mA / div.
 Lower: V_{IN} , 200 V, 5 ms / div.

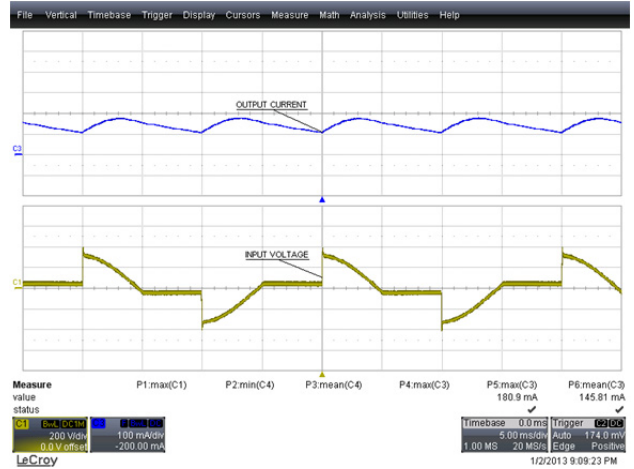


Figure 62 – 90° Conduction Angle.
 Upper: I_{OUT} , 100 mA / div.
 Lower: V_{IN} , 200 V, 5 ms / div.

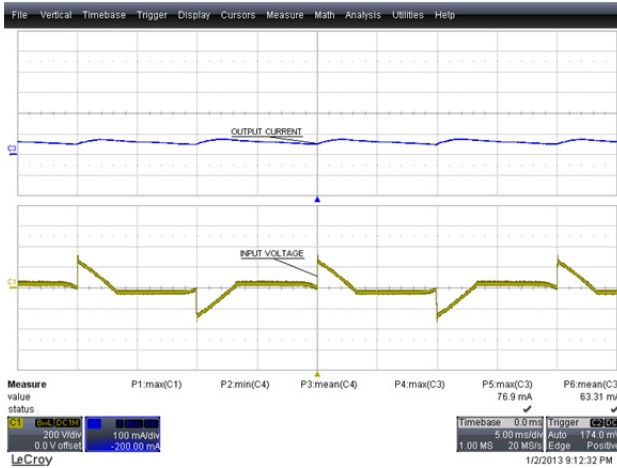


Figure 63 – 60° Conduction Angle.
 Upper: I_{OUT} , 100 mA / div.
 Lower: V_{IN} , 200 V, 5 ms / div.

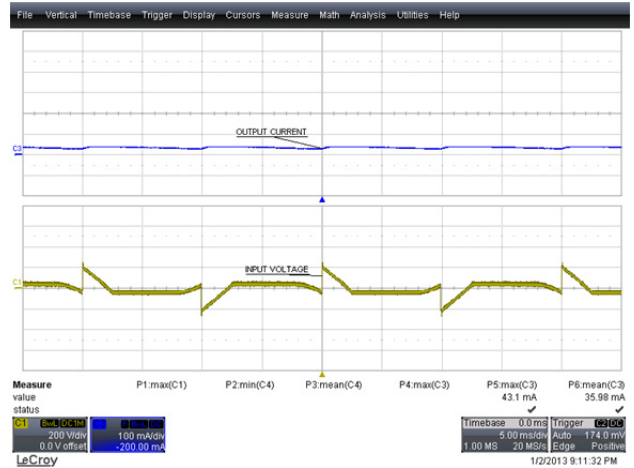


Figure 64 – 45° Conduction Angle.
 Upper: I_{OUT} , 100 mA / div.
 Lower: V_{IN} , 200 V, 5 ms / div.



14 Conducted EMI

14.1 Test Set-up

The unit was tested using LED load ($\sim 41\text{ V } V_{\text{OUT}}$) with input voltage of 230 VAC, 60 Hz at room temperature.



Figure 65 – EMI Test Set-up with the Unit and LED Load Placed Inside the Cone.



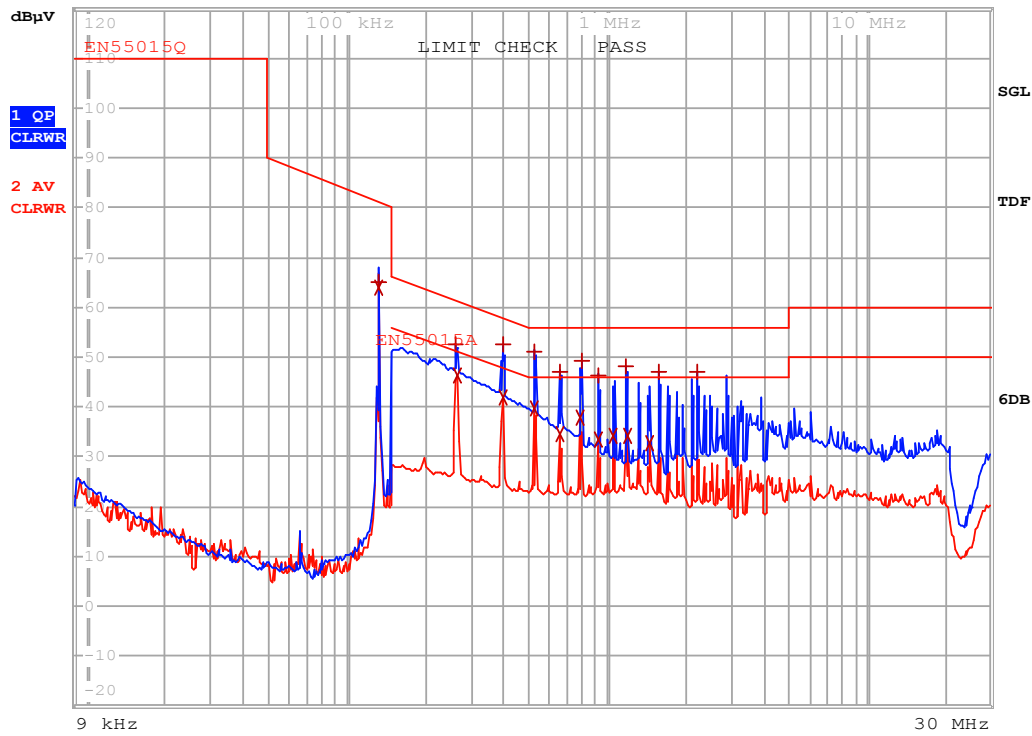
13.2 Test Result



Power Integrations
28.Dec 12 19:36

RBW 9 kHz
MT 500 ms

Att 10 dB AUTO



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE	FREQUENCY	LEVEL dBµV	DELTA	LIMIT dB
1 Quasi Peak	132.133649648 kHz	64.88	L1 gnd	-16.27
2 Average	132.133649648 kHz	64.05	N gnd	
1 Quasi Peak	261.871472881 kHz	52.59	N gnd	-8.77
2 Average	264.49018761 kHz	46.39	N gnd	-4.89
1 Quasi Peak	393.789848222 kHz	52.43	L1 gnd	-5.54
2 Average	397.727746704 kHz	41.86	L1 gnd	-6.03
1 Quasi Peak	525.514079005 kHz	51.18	L1 gnd	-4.81
2 Average	525.514079005 kHz	39.64	N gnd	-6.35
1 Quasi Peak	654.11570866 kHz	47.19	L1 gnd	-8.80
2 Average	660.656865747 kHz	34.39	N gnd	-11.60
2 Average	790.243042258 kHz	37.93	L1 gnd	-8.06
1 Quasi Peak	798.145472681 kHz	49.25	L1 gnd	-6.74
1 Quasi Peak	917.447639259 kHz	46.18	L1 gnd	-9.81
2 Average	917.447639259 kHz	33.50	N gnd	-12.49
2 Average	1.05458240332 MHz	34.23	L1 gnd	-11.76
1 Quasi Peak	1.17656420634 MHz	48.27	L1 gnd	-7.72
2 Average	1.1883298484 MHz	34.09	L1 gnd	-11.90
2 Average	1.44998824519 MHz	32.56	L1 gnd	-13.43
1 Quasi Peak	1.57012949439 MHz	47.22	L1 gnd	-8.77
1 Quasi Peak	2.22424976908 MHz	47.16	L1 gnd	-8.83

Figure 66 – Conducted EMI, 41 V LED Load, 230 VAC, 60 Hz, and EN55015 B Limits.



15 Line Surge Test

The unit was subjected to ± 2500 V, 100 kHz ring wave and ± 500 V differential surge at 230 VAC using 10 strikes at each condition. A test failure was defined as a non-recoverable interruption of output requiring supply repair or recycling of input voltage.

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass
+2500	230	L1, L2	0	100 kHz Ring Wave (500 A)	Pass
-2500	230	L1, L2	90	100 kHz Ring Wave (500 A)	Pass

Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Type	Test Result (Pass/Fail)
+500	230	L1, L2	0	Surge (2Ω)	Pass
-500	230	L1, L2	90	Surge (2Ω)	Pass
+500	230	L1, L2	0	Surge (2Ω)	Pass
-500	230	L1, L2	90	Surge (2Ω)	Pass

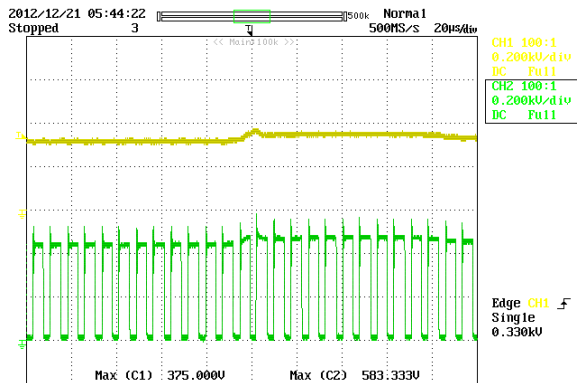


Figure 67 – (+)500 V Differential Surge, 90°. Upper: V_{BULK} , 200 V / div. Lower: V_{DRAIN} , 200 V, 20 μ s / div.

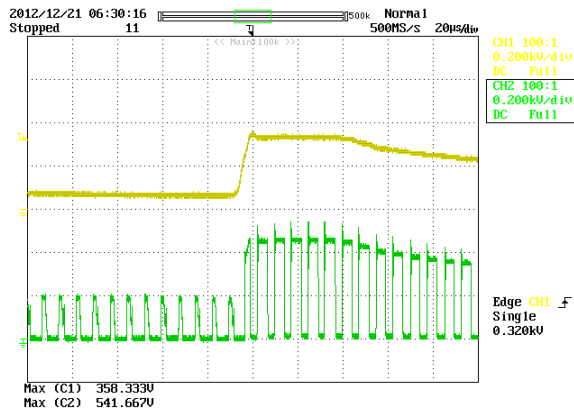


Figure 68 – (+)500 V Differential Surge, 0°. Upper: V_{BULK} , 200 V / div. Lower: V_{DRAIN} , 200 V, 20 μ s / div.



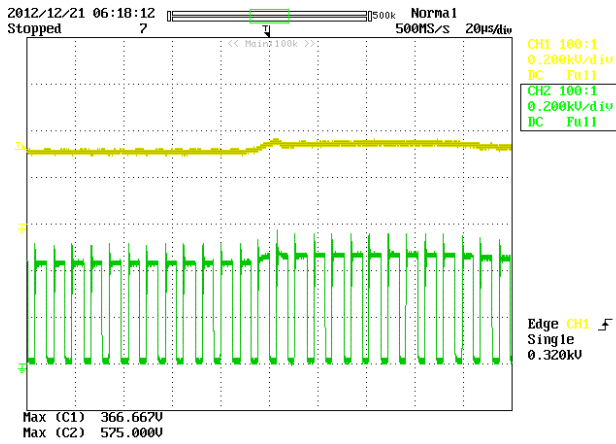


Figure 69 – (-)500 V Differential Surge, 90°. Upper: V_{BULK} , 200 V / div. Lower: V_{DRAIN} , 200 V, 20 μ s / div.

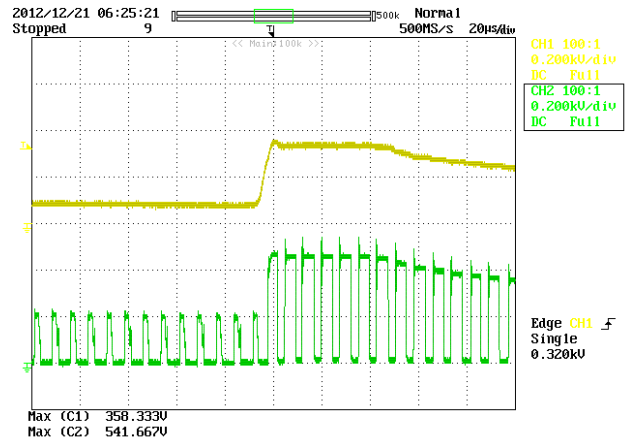


Figure 70 – (-)500 V Differential Surge, 0°. Upper: V_{BULK} , 200 V / div. Lower: V_{DRAIN} , 200 V, 20 μ s / div.

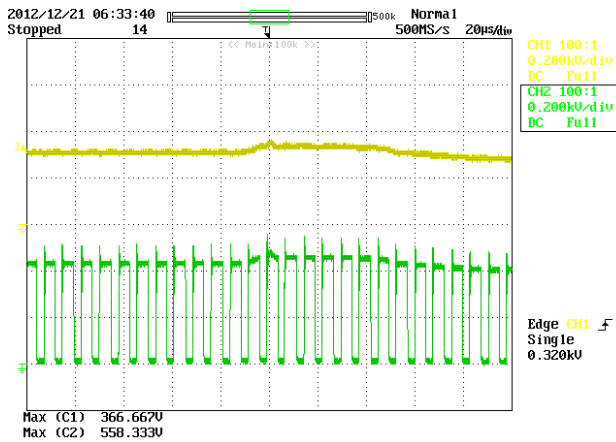


Figure 71 – (+)2.5 kV Ring Wave, 90°. Upper: V_{BULK} , 200 V / div. Lower: V_{DRAIN} , 200 V, 20 μ s / div.

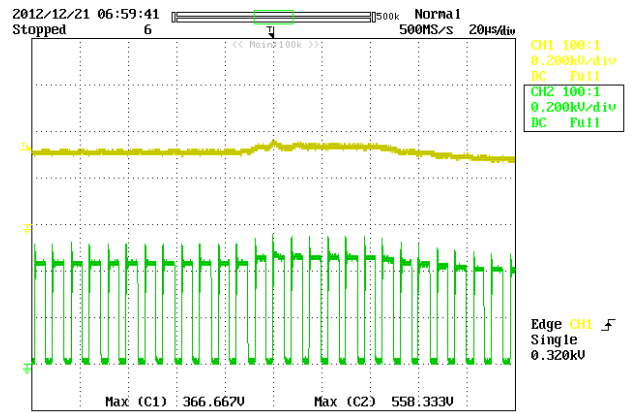


Figure 72 – (-)2.5 kV Ring Wave, 90°. Upper: V_{BULK} , 200 V / div. Lower: V_{DRAIN} , 200 V, 20 μ s / div.



16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
15-May-13	DS	1.0	Initial Release	Apps & Mktg



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