Design Example Report

Title	***15W Multiple Output DC-DC Forward Converter with Synchronous Rectification using DPA424P***
Specification	Input: 36 - 72 VDC Output: 5V / 2.4A, 7.5V / 0.4A, 20V / 10mA
Application	IP Phone
Author	Power Integrations Applications Department
Document Number	DER-24
Date	March 30, 2004
Revision	1.0

Summary and Features

This report describes a design for a DC-DC power supply, such as required for an IP phone, featuring the following:

- High Overall Power Supply Efficiency (88% at 48 VDC with DPA424)
- Self-driven Synchronous Rectification
- 400kHz Operation
- Good fit for VoIP applications

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolated source to provide power to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.

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1 Introduction

This document is an engineering report describing a DC-DC Forward converter with three outputs using the DPA424R. The input voltage range is 36 to 72 VDC providing outputs 5 V/7.5 V/20 V at 15 W. The power supply achieves approximately 88% efficiency with synchronous rectification. The supply uses a coupled output inductor to provide the voltage outputs.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

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2 Power Supply Customer Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	36		72	V_{DC}	Turn-on –33V+-2.5V, Turn-off -86V +-2.5V
No-load Input Power			-		W	
Overload Input Current			-		A	Maximum allowed input current
Output1						
Output Voltage 1	V_{OUT1}	4.75	5.0	5.25	V	± 3%
Output Ripple Voltage 1	$V_{RIP1P-P}$		110		mVp-p	20 MHz Bandwidth
Output Current 1	I_{OUT1}	0.5		2.4	A	
Output Voltage 2	V_{OUT2}	7.1	7.50	8.25	V	-5 +10%
Output Ripple Voltage 2	$V_{RIP2P-P}$		100		mVp-p	20 MHz Bandwidth
Output Current 2	I_{OUT2}	0		0.4	A	
Output Voltage 3	V_{OUT3}	19.5	20.0	21.5	V	-2.5 +7.5%
Output Ripple Voltage 3	$V_{RIP3P-P}$		180		mVp-p	20 MHz Bandwidth
Output Current 3	I_{OUT3}	0.01		0.01	A	
Total Output Power						
Continuous Output Power	P_{OUT}			15	W	
Peak Output Power	P_{OUT_PEAK}		-		W	
Efficiency	η		88	89	%	
Input-Output Isolation Voltage		1500			V_{DC}	
Ambient Temperature	T_{AMB}	-5	25	55	^{o}C	Free convection, Sea level

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3 Schematic

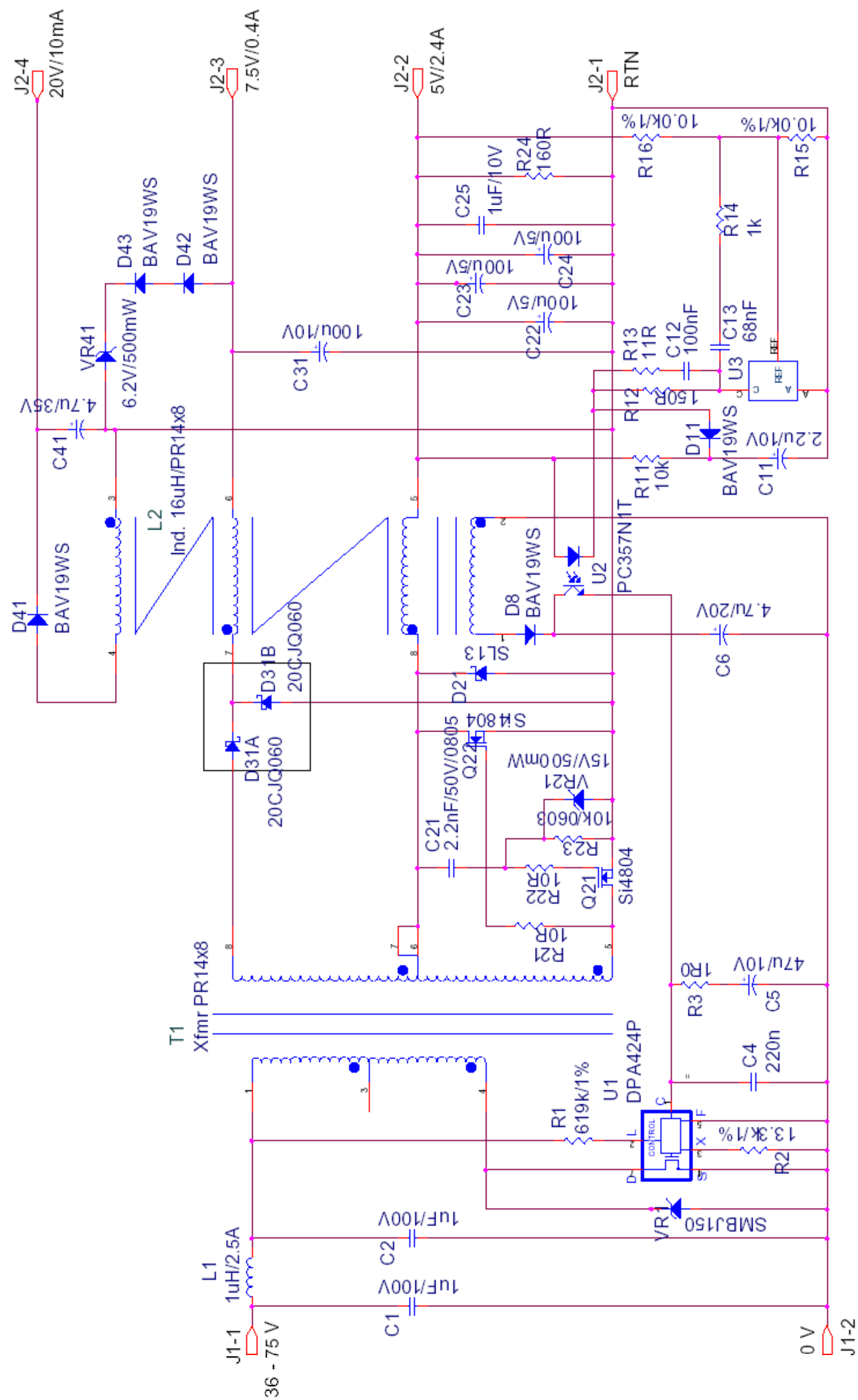

Figure 1 – Schematic

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4 Circuit Description

The circuit shown is a single output DC-DC Forward power supply using the DPA424. This circuit uses both synchronous rectification and a coupled output inductor in order to meet power supply specifications.

4.1 Input EMI filtering

Components C1,C2 and L1 filter conducted emissions from the power supply.

4.2 Power Supply Primary

Resistor R1 programs the under-voltage and over-voltage thresholds for the DPA-Switch. Resistor R2 programs the device current limit (which determines the amount of power delivered in an over-load condition). Capacitor C4 provides device de-coupling and components C5 and R3 are part of the feedback compensation (C5 also determines the auto-restart period of the device). Components D8 and C6 rectify and filter the bias-supply voltage and opto-transistor U2 feeds back the signal from the secondary side. Zener diode VR1 clamps the maximum drain voltage to a safe level during fault conditions (it is not active during normal switching).

The transformer T1 provides voltage conversion from the primary and feeds from two windings into the secondary coupled inductor. Diodes D31A and D31B feed the 7.5V inductor winding, and synchronous rectifier MOSFETS Q21 and Q22 feed the 5V inductor winding. Synchronous rectification is driven passively from the transformer windings. Capacitor C21 charges the gate of Q21 through resistor R22. Zener diode VR21 limits the forward voltage on the gate of Q21 (forward sync-MOSFET) and during the Q21 off time, provides a path for discharge of capacitor C21. Resistor R23 ensures that Q21 remains off when there is no switching signal. The reset energy of the transformer T1, drives through resistor R21 to the gate of Q22 (Catch sync-MOSFET) during the primary off-time. Diode SL13 provides a continuous conduction path for the catch period, after the reset of the transformer is complete.

The 20 V output is implemented with a flyback winding on the coupled inductor. This winding is rectified by diode D41 and a voltage offset from the 7.5 V winding, is provide by components VR41, D43 and D42. The output is filtered by capacitor C41. Likewise the output of 7.5 V is filtered by capacitor C31 and the 5 V output is filtered by C22, C23, C24, C25. Resistor R24 provides a small pre-load to improve no-load regulation.

Resistors R16 and R15 sense the 5 V output voltage and feed a signal to the TL431 U3. Components C13 and R14 compensate to reduce the high frequency gain of the TL431. Components R13 and C12 provide phase-lead compensation to improve phase-margin at high frequency. Opto-diode U2 is connected from the 5 V output to resistor R12 , this resistor programs the gain of the feedback circuit. Components R11, D11 and C11 implement a soft-finish circuit, which eliminates overshoot during power supply start-up.

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5 PCB Layout

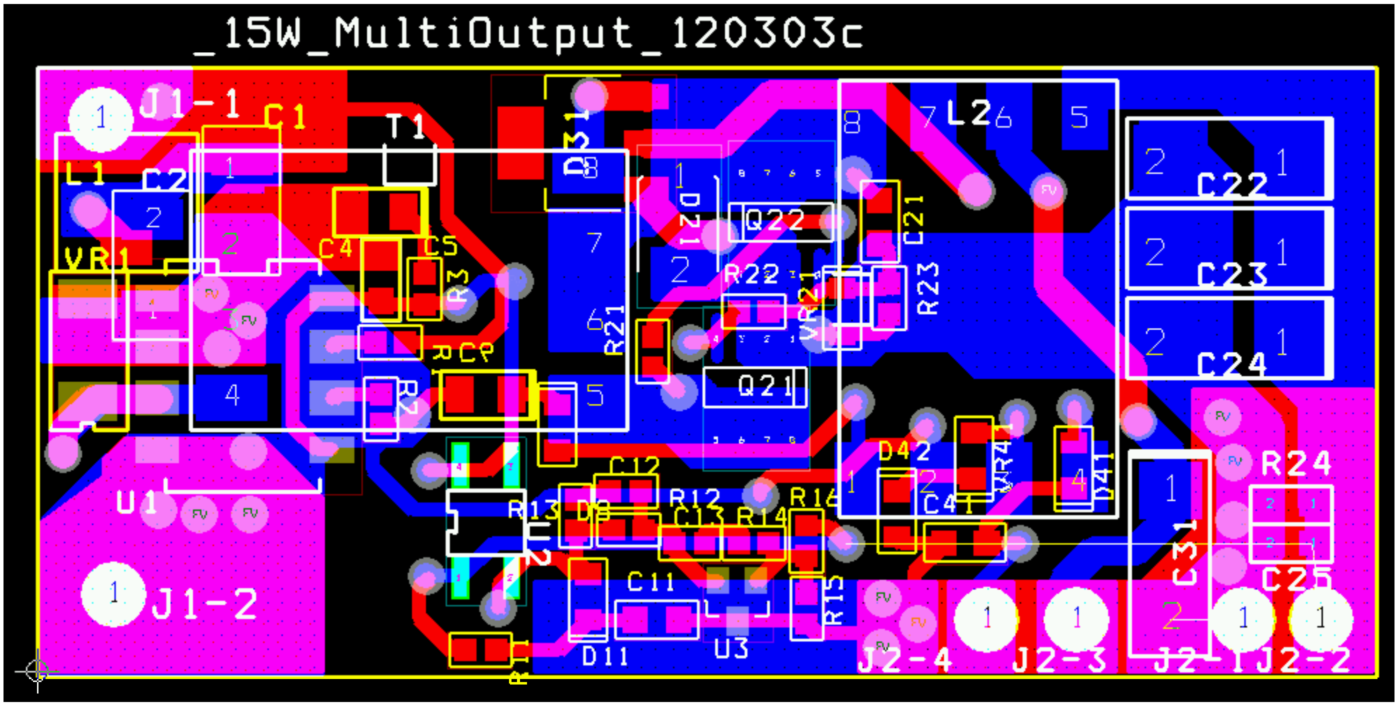

Figure 2 – Printed Circuit Layout.

6 Bill Of Materials

6.1 Main Converter

15W MultiOutput 121003A

Item	Qty	Reference	Description	P/N	Manufacturer
1	1	C1	1uF/100V		
2	1	C2	1uF/100V		
3	1	C4	220n		
4	1	C5	47u/10V		
5	1	C6	4.7u/20V		
6	1	C11	2.2u/10V		
7	1	C12	100nF		
8	1	C13	68nF		
9	1	C21	2.2nF/50V/0805		
10	1	C22	100u/5V		
11	1	C23	100u/5V		
12	1	C24	100u/5V		
13	1	C25	1uF/10V		
14	1	C31	100u/10V		

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15	1	C41	4.7u/35V
16	1	D8	BAV19WS
17	1	D11	BAV19WS
18	1	D21	SL13
19	1	D41	BAV19WS
20	1	D42	BAV19WS
21	1	D43	BAV19WS
22	1	D31	20CJQ060
23	1	L1	1uH/2.5A
24	1	L2	Ind. 16uH/PR14x8
25	1	Q21	Si4804
26	1	Q22	Si4804
27	1	R1	619k/1%
28	1	R2	13.3k/1%
29	1	R3	1R0
30	1	R11	10k
31	1	R12	150R
32	1	R13	11R
33	1	R14	1k
34	1	R15	10.0k/1%
35	1	R16	10.0k/1%
36	1	R21	10R
37	1	R22	10R
38	1	R23	10k/0603
39	1	R24	160R
40	1	T1	Xfmr PR14x8
41	1	U1	DPA424P
42	1	U2	PC357N1T
43	1	U3	U3
44	1	VR1	SMBJ150
45	1	VR21	15V/500mW
46	1	VR41	6.2V/500mW

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7 Transformer - T1 Rev 121003a

7.1 Electrical Diagram

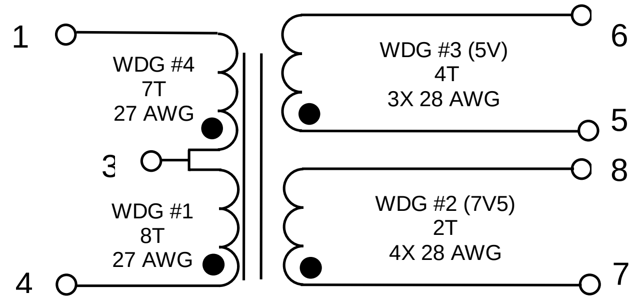

Figure 3 –Transformer Electrical Diagram

7.2 Electrical Specifications

Electrical Strength	1 second, from Pins 1-4 to Pins 5-8	1500 VDC
Primary Inductance	Pins 1,4, all other windings open, measured at 100KHz, 400mVRMS	434 uH, ±25 %
Resonant Frequency	Pins 1-4, all other windings open	3.8 MHz (Min.)
Primary Leakage Inductance	Pins 1-4, with Pins 5-8 shorted, measured at 100KHz, 400mVRMS	1 uH (Max.)

7.3 Materials

Item	Description
[1]	Core: PR 14 X 8 **Ungapped** 3F3 Material Philips/Ferroxcube P/N PTS14/8-3F3
[2]	Bobbin: 8 pin P1408 surface mount B&B B-096 or equivalent
[3a]	Magnet Wire: #27 AWG Double Coated
[3b]	Magnet Wire: #28 AWG Double Coated
[4]	Tape, Polyester, 3M #1298 or equiv. 4.5mm wide
[5]	Varnish

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7.4 Transformer Build Diagram

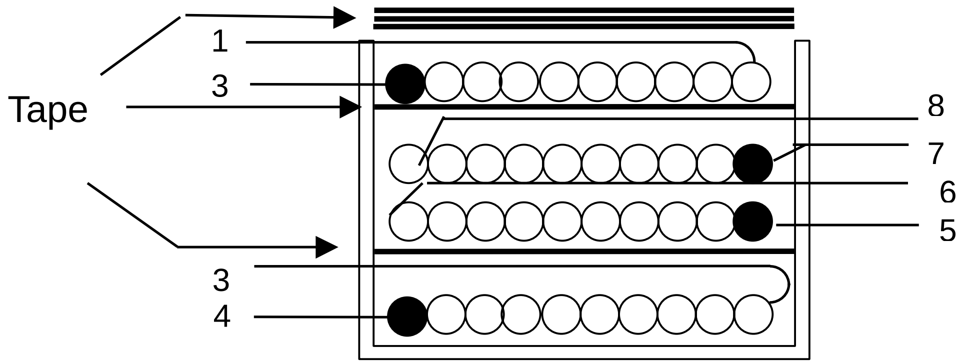

Figure 4 – Transformer Build Diagram

7.5 Transformer Construction

Wdg #1	Start at Pin 4. Wind 8 turns of item [3a] in 1 layer. Finish on FL
Basic Insulation	Use one layer of item [4] for basic insulation.
Wdg #2	Start at Pin 7. Wind 2 quadrifilar turns of item [3b] Finish on Pin 8.
Wdg #3	Start at Pin 5. Wind 4 trifilar turns of item [3b] Finish on Pin 6.
Basic Insulation	Use one layer of item [4] for basic insulation.
Wdg #4	Start at FL. Wind 7 turns of item [3a] in 1 layer. Finish on Pin 1.
Outer Wrap	Wrap windings with 2 layers of tape item [4].
Final Assembly	Tape around to secure cores.

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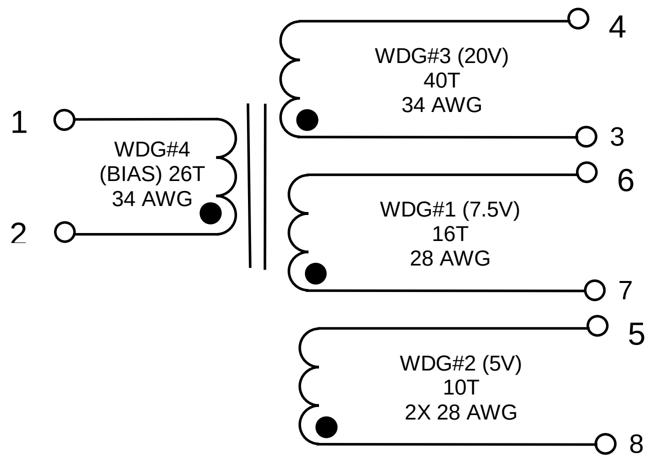
8 Inductor – Rev L2 121003A



8.1 Electrical Specifications

Electrical Strength	1 second, from Pins 1,2 to Pins 5-8	1500 VDC
Inductance	Pins 3-4, all other windings open, measured at 100KHz, 400 mVRMS	16 uH, ±10 %
Resonant Frequency		N/A
Primary Leakage Inductance		N/A

8.2 Materials

Item	Description
[1]	Core: PR 14 X 8 Epcos N87, P/N B65755-J-R87 Gap for AL of 160 nH/T2
[2]	Bobbin: 8 pin P1408 surface mount B&B B-096 or equivalent
[3]	Magnet Wire: #28 AWG Double Coated
[4]	Magnet Wire: #34 AWG Double Coated
[5]	Tape, Polyester, 3M #1298 or equiv. 4.5mm wide
[6]	Varnish

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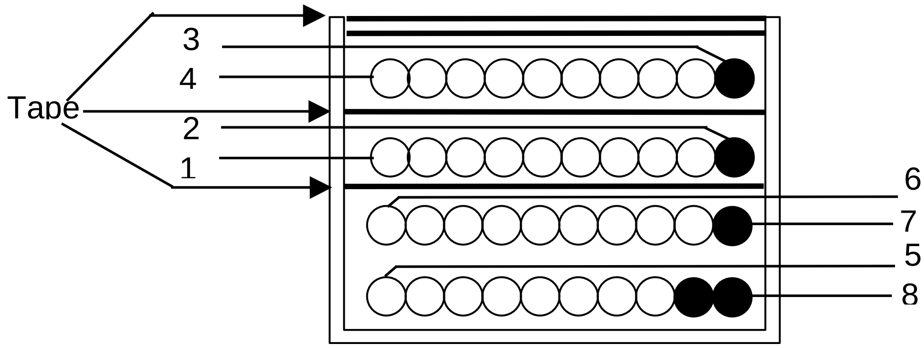
8.3 Inductor Build Diagram



WINDING INSTRUCTIONS:

Wdg #1	Start at Pin 7. Wind 16 turns of item [3] Finish on Pin 6.
Wdg #2	Start at Pin 8. Wind 10 bifilar turns of item [3] Finish on Pin 5
Basic Insulation	Use one layer of item [5] for basic insulation.
Wdg #3	Start at Pin 3. Wind 40 turns of item [4] Finish on Pin 4.
Basic Insulation	Use one layer of item [5] for basic insulation.
Wdg #4	Start at Pin 2. Wind 26 turns of item [4] in approximately 1 layer. Finish on Pin 1.
Outer Wrap	Wrap windings with 3 layers of tape [item [5].

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9 Transformer Spreadsheets

DCDC_DPAFwd_rev1.03_092702 Copyright Power Integrations Inc. 2002	INPUT	INFO	OUTPUT	UNIT	DPA_092702_R102xls: DPA-Switch Forward Transformer Design Spreadsheet
OUTPUT VOLTAGE AND CURRENT					DI-32 - 15W multioutput 5V2.4A 7.5V0.4A 20V0.01A
VMAIN	5			Volts	Main output voltage
IMAIN	3.04			Amps	Main output current
VOUT2				Volts	Output2 voltage
IOUT2				Amps	Output2 current
POUT			15.2	Watts	Total output power
VBIAS	12.0			Volts	DC bias voltage from output inductor winding
INPUT VOLTAGE AND UV/OV					
VMIN	36			DC volts	Minimum DC input voltage
VMAX	72			DC volts	Maximum DC input voltage
		min	max		
VUV OFF		29.34	32.35573	DC volts	Minimum undervoltage On-Off threshold
VUV ON		31.45101	33.8636	DC volts	Maximum undervoltage Off-On threshold (turn-on)
VOV ON		73.06809	-	DC volts	Minimum overvoltage Off-On threshold
VOV OFF		-	92.36876	DC Volts	Maximum overvoltage On-Off threshold (turn-off)
RL			603.1461	kOhm	Line Sense resistor value (L-pin) - goal seek (VUV OFF) for std 1% resistor series
ENTER DPA-Switch VARIABLES					
DPA-Switch	**dpa424**			16VDC	36VDC
Chosen Device	*#N/A*		Power	15.5W	35W
ILIMIT	*#REF!*	2.68		Amps	From DPA-Switch datasheet
Frequency - (F)=400k	**f**				Full (F) frequency option - 400kHz
fS	*#REF!*	425000	400000	Hertz	From DPA-Switch datasheet
KI	0.5				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITEXT			1.16	Amps	External current limit. Use 1% resistor to set current limit
RX			13.37988	kOhm	Current Limit resistor value (X-pin) - assumes minimum datasheet curve (fig 32)
DUVON GOAL	0.65		0.65		Maximum allowed duty cycle at VUV ON MIN undervoltage threshold
KDI	0.19		0.19		Maximum current ripple factor
VDS			1	Volts	DPA-Switch average on-state Drain to Source Voltage
VDSOP			174.6585	Volts	Required drain voltage for guaranteed transformer reset
DIODE Vf SELECTION					
VDMAIN	0.1		0.1	Volts	Main output diodes forward voltage drop
VDOUT2			0.5	Volts	Secondary output diodes forward voltage drop
VDB			0.7	Volts	Bias diode forward voltage drop
TRANSFORMER CORE SELECTION					
Core Type	**pr14x8**				
Core		PR14x8		P/N:	B65755-J-R87
Bobbin		PR14x8_B		P/N:	B65542-B-T1
AE			0.253	cm^2	Core Effective Cross Sectional Area
LE			2.53	cm	Core Effective Path Length
AL			2000	nH/T^2	Ungapped Core Effective Inductance
BW			4.4	mm	Bobbin Physical Winding Width
LG MAX			0.002	mm	Maximum actual gap when zero gap specified
D FACTOR			1		Duty cycle factor
L	1.00				Transformer primary layers (split primary recommended)
NMAIN			4		Main rounded turns
NS2			0		Vout2 rounded secondary turns (AC stacked winding)
VOUT2 ACTUAL			0	Volts	Approximate Output2 voltage of with NS2 = 0 turns (AC stacked secondary)

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TRANSFORMER DESIGN PARAMETERS					
NP			15		Primary rounded turns
BM			1343.874	Gauss	Max operating flux density at minimum switching frequency
BP			2728.903	Gauss	Max transient flux density at minimum switching frequency
LP MIN			0.399711	mHenries	Minimum primary magnetizing inductance (assumes LG MAX=2um)
IMAG			0.119618	Amps	Peak magnetizing current at minimum input voltage
OD_P			0.345095	mm	Primary wire outer diameter
AWG_P			28	AWG	Primary Wire Gauge (rounded to maximum AWG value)
DUTY CYCLE VALUES					
DUVON MIN			0.628058		Duty cycle at minimum undervoltage threshold
DVMIN			0.546429		Duty cycle at minimum DC input voltage
DVMAX			0.269366		Duty cycle at minimum DC input voltage
DOVOFF MAX			0.209317		Duty cycle at maximum DC overvoltage threshold
CURRENT WAVESHAPE PARAMETERS					
IP			0.946646	Amps	Maximum peak primary current at maximum DC input voltage
IPRMS			0.599251	Amps	Maximum primary RMS current at minimum DC input voltage
COUPLED INDUCTOR OUTPUT PARAMETERS					
LMAIN			16.12808	uHenries	Main / Output2 coupled output inductance (referred to Main winding)
WLMAIN			74.52466	uJoules	Main / Output2 coupled output inductor full-load stored energy
KDIMAIN			0.19		Current ripple factor of combined Main and Output2 outputs
nOUT2			0		Approximate turns ratio for Output2 winding
nBIAS			2.490196		Approximate turns ratio for Bias winding
SECONDARY OUTPUT PARAMETERS					No derating
ISMAINRMSLL			2.247193	Amps	Maximum transformer secondary RMS current (AC stacked secondary)
ISOUT2RMSLL			0	Amps	Maximum transformer secondary RMS current (AC stacked secondary)
IDAVMAIN			2.221127	Amps	Maximum average current, Main rectifier (single device rating)
IDAVOUT2			0	Amps	Maximum average current, Main rectifier (single device rating)
IRMSMAIN			0.166739	Amps	Maximum RMS current, Main output capacitor
IRMSOUT2			0	Amps	Maximum RMS current, Out2 output capacitor
VPIVMAIN			38.75159	Volts	Main rectifiers peak-inverse voltage
VPIVOUT2			0	Volts	Output2 rectifiers peak-inverse voltage
VPIVB			58.08	Volts	Bias output rectifier peak-inverse voltage

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10 Performance Data

All measurements performed at room temperature, DC input.

10.1 Efficiency

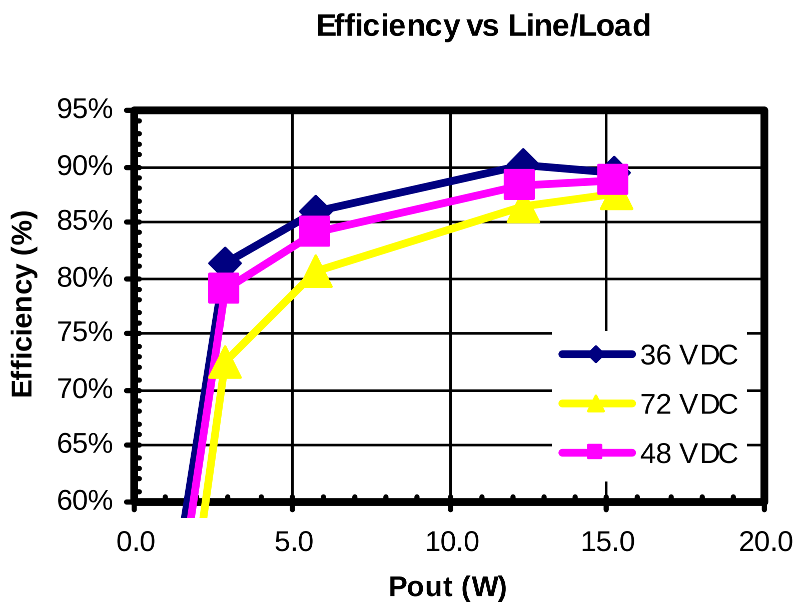

Figure 5- Efficiency vs. Load, Room Temperature.

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10.2 Regulation

10.2.1 Load Regulation

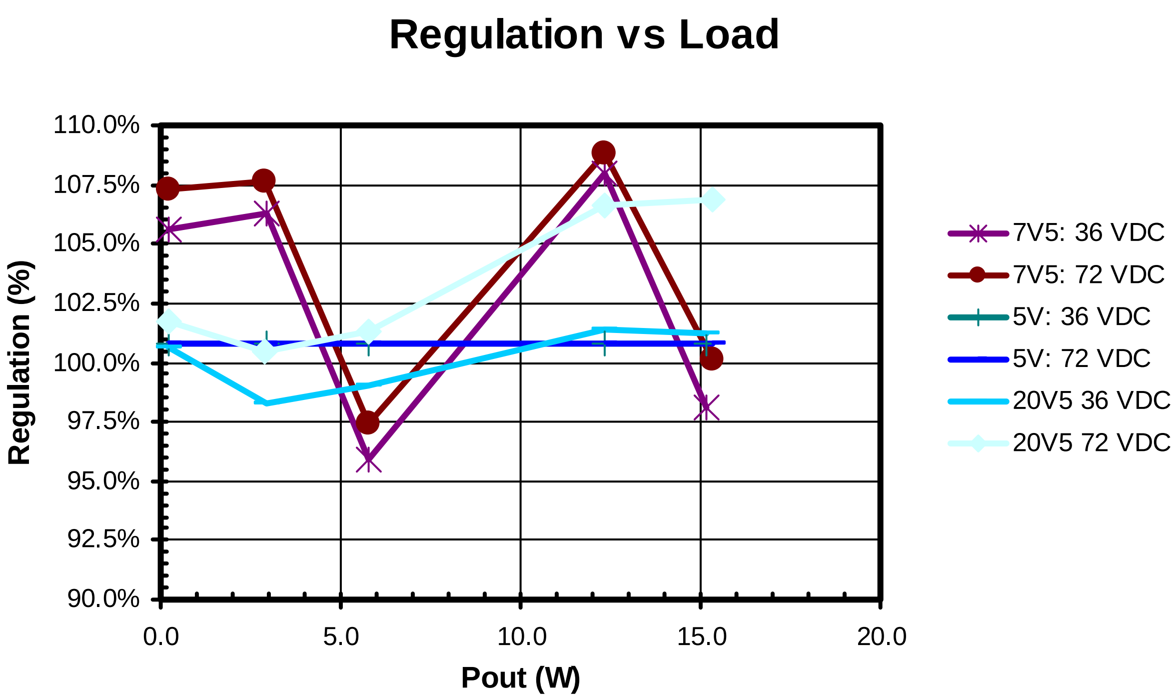

Figure 6 –Load Regulation, 5V,7.5V, 20V, Room Temperature

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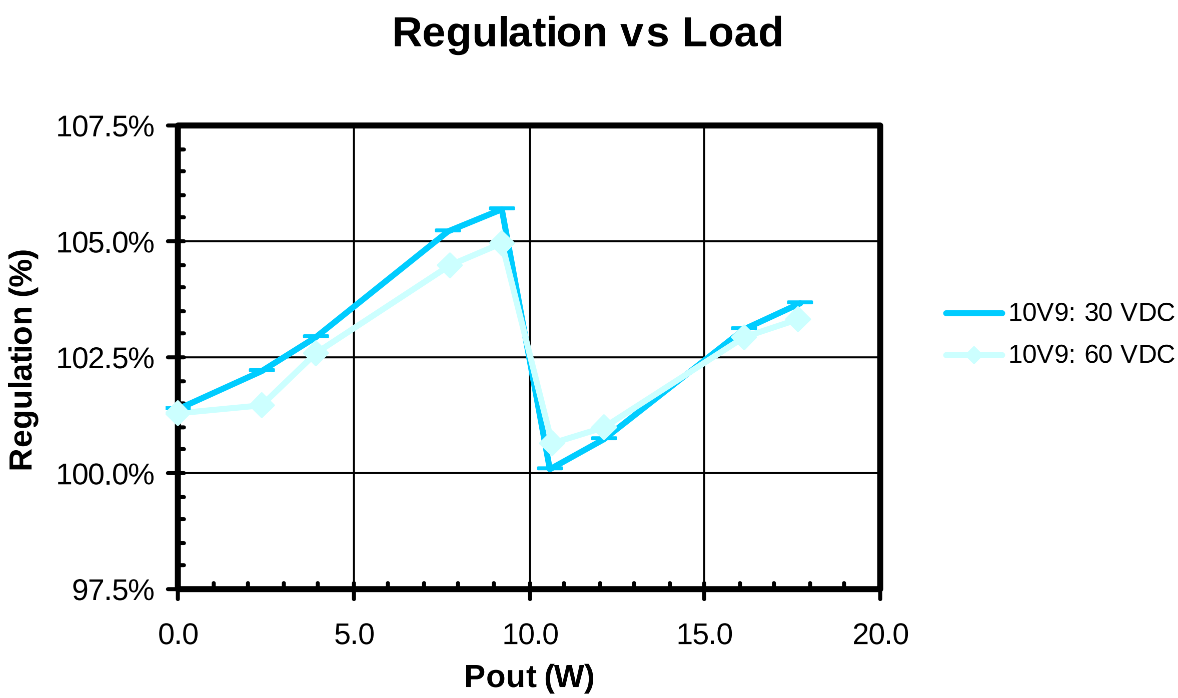

Figure 7 –Load Regulation, 10V9, Room Temperature

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10.2.2 Line Regulation

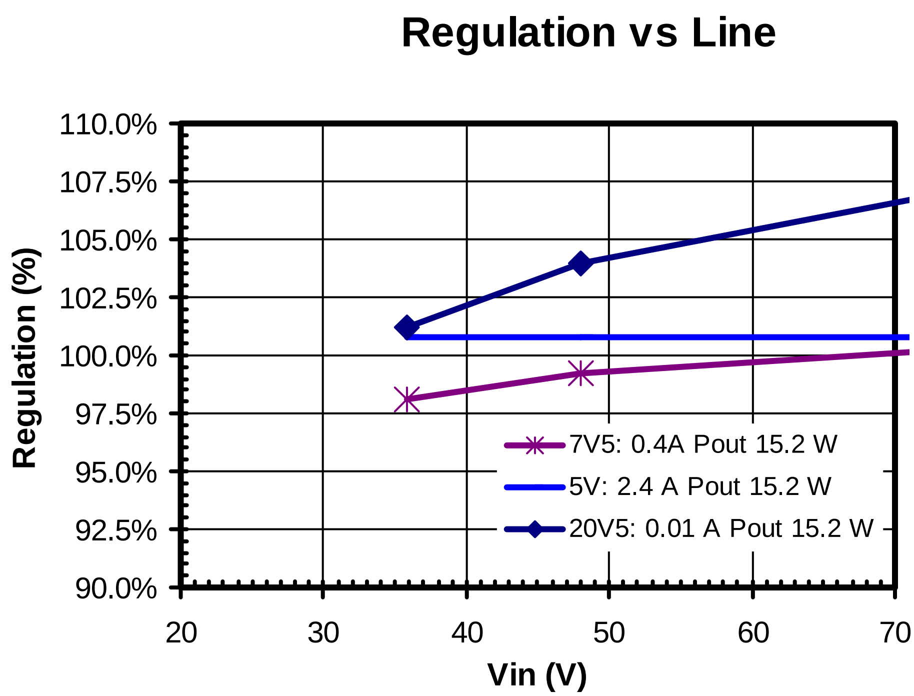

Figure 8 – Line Regulation, Room Temperature, Full Load.

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10.3 Miscellaneous Performance

10.3.1 Overload Performance

Vin	Iin	Iout1	Iout2	Iout3	Pin	Pout
35.8	0.721	4.5	0	0	25.8118	22.5
48.5	0.553	4.63	0	0	26.8205	23.15
72	0.404	4.98	0	0	29.088	24.9

10.3.2 Under-voltage/Over-voltage Performance

Vin	UV	OV
On	30.4	82
Off	33.1	86

10.3.3 Line/Load Test Conditions

Vin	Iin	Vout1	Iout1	Vout2	Iout2	Vout3	Iout3
35.9	0.017	5.04	0	7.92	0	20.13	0.01
35.9	0.1	5.04	0.54	7.97	0	19.65	0.01
35.9	0.188	5.04	0.54	7.19	0.4	19.81	0.01
35.8	0.383	5.04	2.41	8.1	0	20.28	0.01
35.8	0.474	5.04	2.39	7.36	0.4	20.25	0.01
48	0.015	5.04	0	7.99	0	20.07	0.01
48	0.077	5.04	0.54	8.01	0	19.75	0.01
48	0.143	5.04	0.53	7.26	0.4	20.03	0.01
48	0.29	5.04	2.4	8.12	0	20.77	0.01
48	0.358	5.04	2.39	7.44	0.4	20.79	0.01
71.9	0.016	5.04	0	8.05	0	20.34	0.01
72	0.055	5.04	0.53	8.07	0	20.1	0.01
72	0.1	5.04	0.53	7.31	0.4	20.26	0.01
71.9	0.198	5.04	2.4	8.16	0	21.33	0.01
72	0.243	5.04	2.39	7.51	0.41	21.37	0.01

Max	**5.04**	0.8%	**8.16**	8.8%	**21.37**	6.9%
Min	**5.04**	0.8%	**7.19**	-4.1%	**19.65**	-1.8%
Delta		0.0%		12.9%		8.6%

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10.3.4 Line/Load Regulation and Efficiency Performance

Vin	Iin	%Vout1	%Vout2	%Vout3	Eff	Pin	Pout
35.9	0.017	100.8%	105.6%	100.7%	33.0%	0.6	0.2
35.9	0.1	100.8%	106.3%	98.3%	81.3%	3.6	2.9
35.9	0.188	100.8%	95.9%	99.1%	85.9%	6.7	5.8
35.8	0.383	100.8%	108.0%	101.4%	90.1%	13.7	12.3
35.8	0.474	100.8%	98.1%	101.3%	89.5%	17.0	15.2
48	0.015	100.8%	106.5%	100.4%	27.9%	0.7	0.2
48	0.077	100.8%	106.8%	98.8%	79.0%	3.7	2.9
48	0.143	100.8%	96.8%	100.2%	84.1%	6.9	5.8
48	0.29	100.8%	108.3%	103.9%	88.4%	13.9	12.3
48	0.358	100.8%	99.2%	104.0%	88.6%	17.2	15.2
71.9	0.016	100.8%	107.3%	101.7%	17.7%	1.2	0.2
72	0.055	100.8%	107.6%	100.5%	72.5%	4.0	2.9
72	0.1	100.8%	97.5%	101.3%	80.5%	7.2	5.8
71.9	0.198	100.8%	108.8%	106.7%	86.5%	14.2	12.3
72	0.243	100.8%	100.1%	106.9%	87.7%	17.5	15.3

Max	**100.8%**	**108.8%**	**106.9%**	**33.0%**	**17.5**	**15.3**
Min	**100.8%**	**95.9%**	**98.3%**	**17.7%**	**0.6**	**0.2**

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

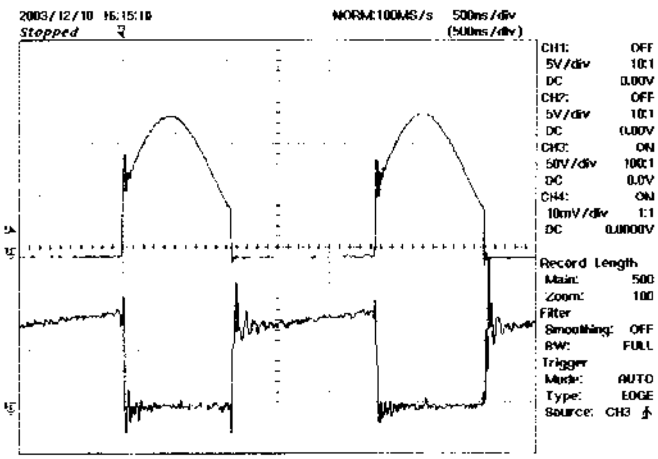

Figure 9 – 36 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{DRAIN}, 50 V/ div
Lower: I_{DRAIN}, 500 mA/ div, 500 ns / div

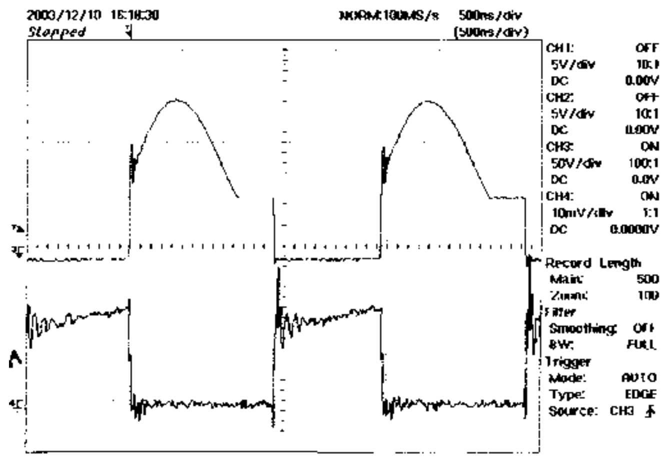

Figure 10– 48 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{DRAIN}, 50 V/ div
Lower: I_{DRAIN}, 500 mA/ div, 500 ns / div

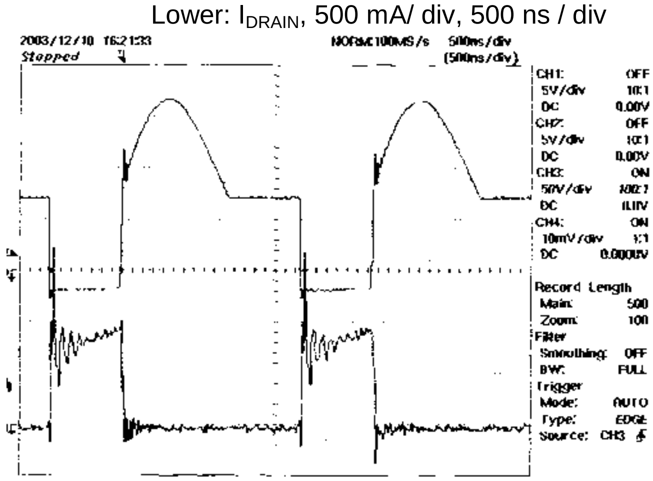

Figure 11 – 72 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{DRAIN}, 50 V/ div
Lower: I_{DRAIN}, 500 mA/ div, 500 ns / div

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11.2 Output Ripple Measurements

11.2.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 12 and Figure 13.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 µF/50 V ceramic type and one (1) 1.0 µF/50 V aluminum electrolytic. *The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).*

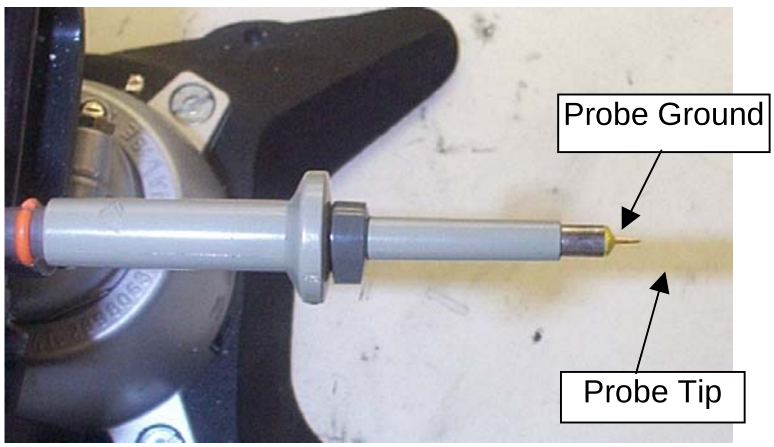

Figure 12 - Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 13 - Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added).

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11.2.2 High Frequency (Switching Ripple) – Measurement Results – 5V Output

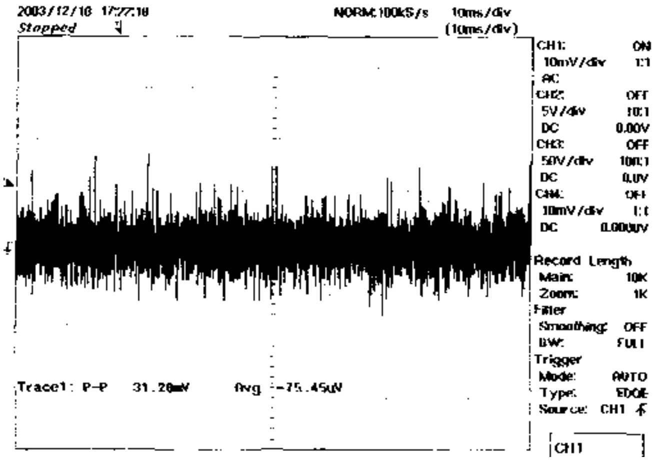

Figure 14 - 36 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{5V}, 10 mV/ div, 1 ms / div

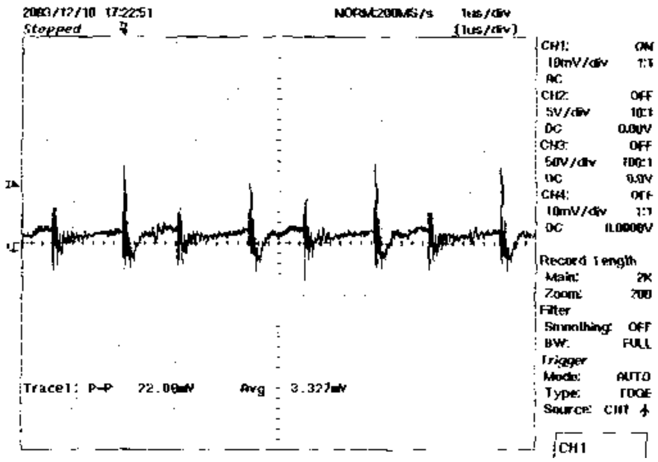

Figure 15 - 36 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{5V}, 10 mV/ div, 1 µs / div

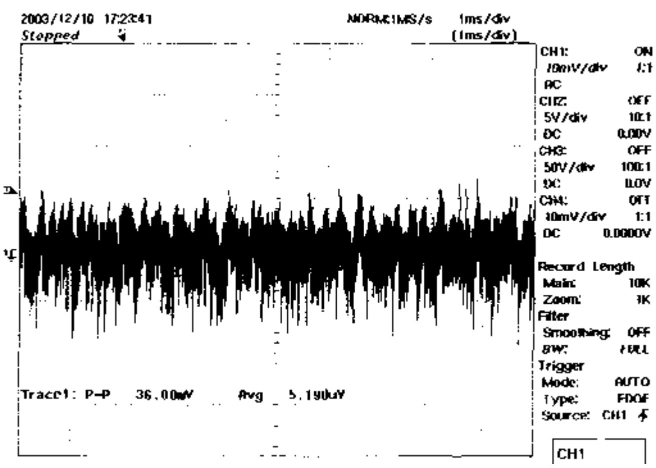

Figure 16 - 48 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{5V}, 10 mV/ div, 1 ms / div

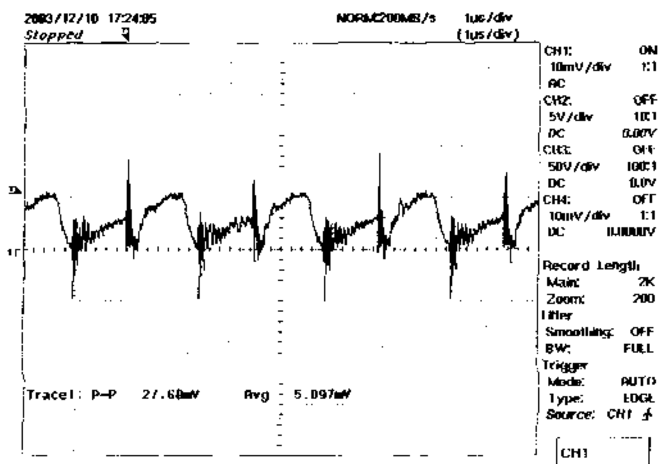

Figure 17 - 48 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{5V}, 10 mV/ div, 1 µs / div

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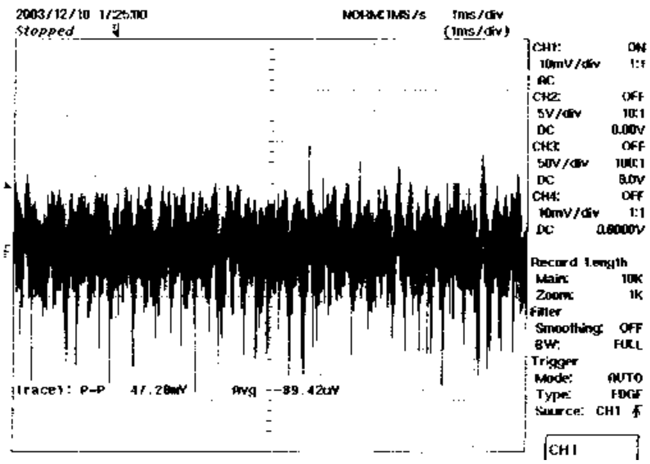

Figure 18 - 72 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{5V}, 10 mV/ div, 1 ms / div

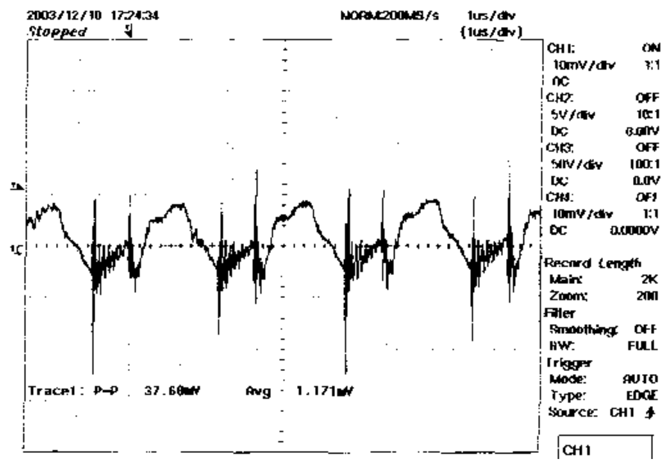

Figure 19 - 72 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{5V}, 10 mV/ div, 1 µs / div

11.2.3 High Frequency (Switching Ripple) – Measurement Results – 7.5V Output

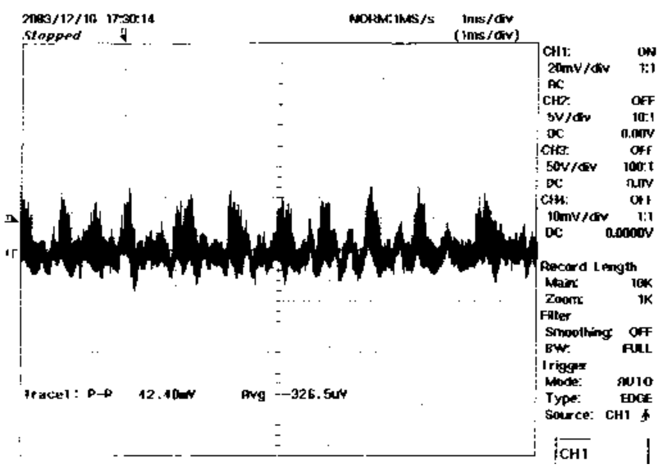

Figure 20 - 36 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: $V_{7.5V}$, 20 mV/ div, 1 ms / div

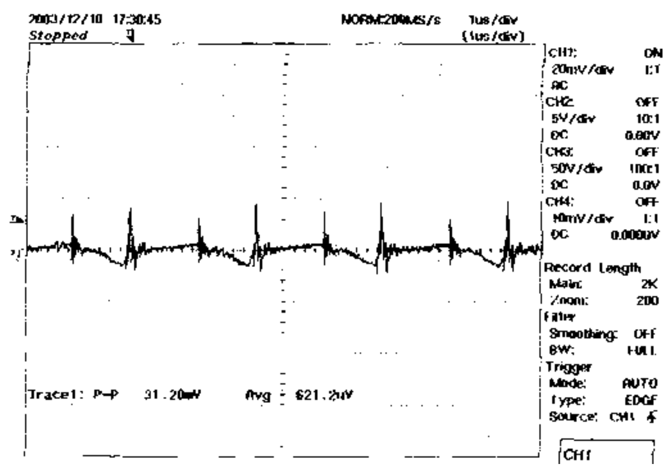

Figure 21 - 36 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: $V_{7.5V}$, 20 mV/ div, 1 µs / div

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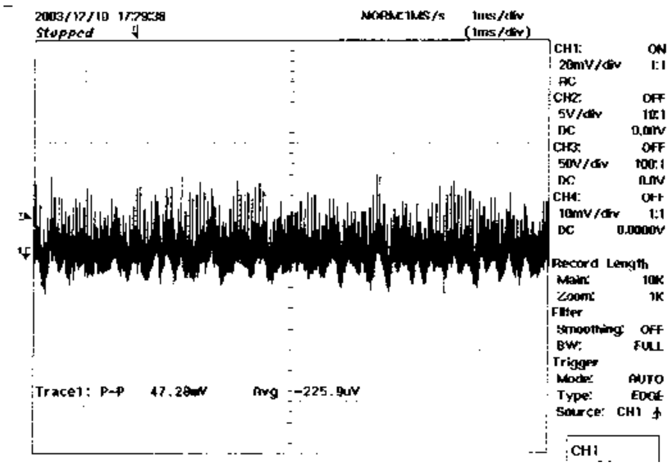

Figure 22 - 48 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: $V_{7.5V}$, 20 mV/ div, 1 ms / div

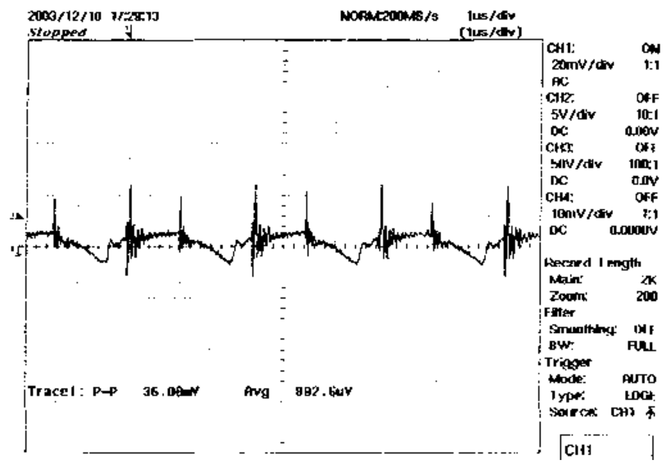

Figure 23 - 48 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: $V_{7.5V}$, 20 mV/ div, 1 µs / div

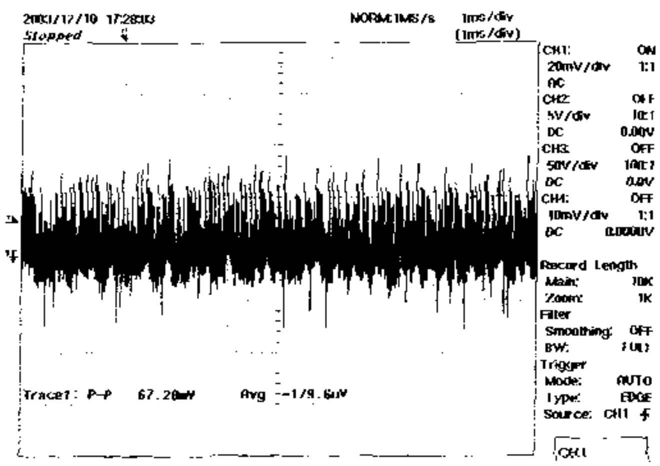

Figure 24 - 72 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: $V_{7.5V}$, 20 mV/ div, 1 ms / div

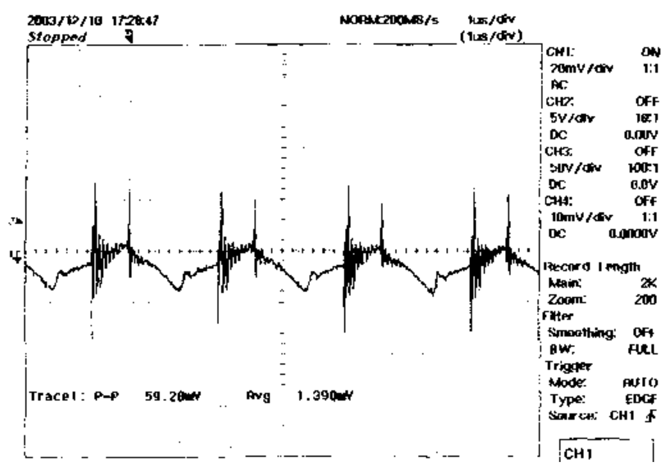

Figure 25 - 72 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: $V_{7.5V}$, 20 mV/ div, 1 µs / div

11.2.4 High Frequency (Switching Ripple) – Measurement Results – 20V Output

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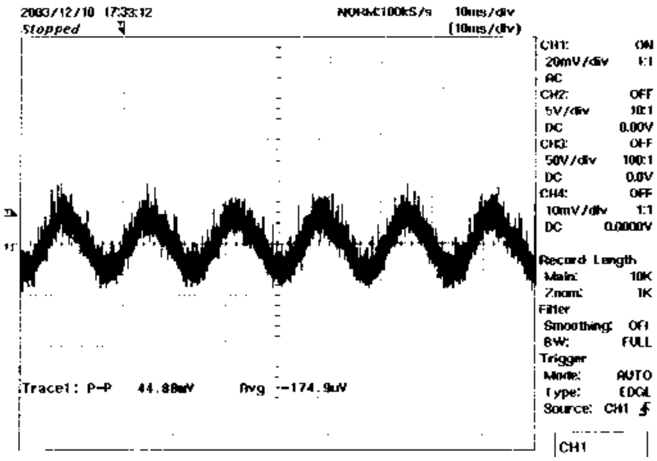

Figure 26 - 36 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{20V}, 20 mV/ div, 1 ms / div

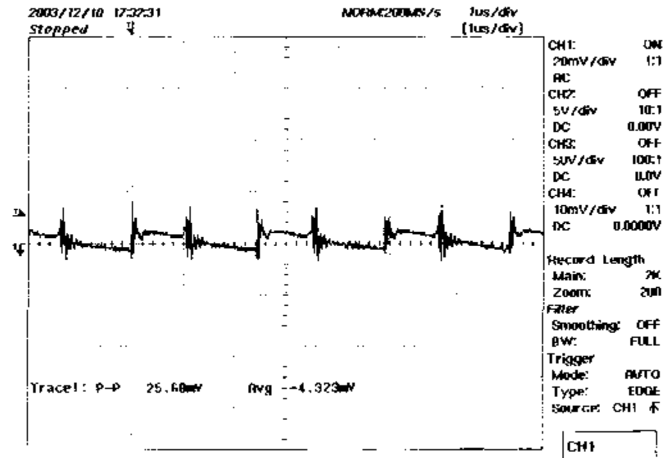

Figure 27 - 36 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{20V}, 20 mV/ div, 1 µs / div

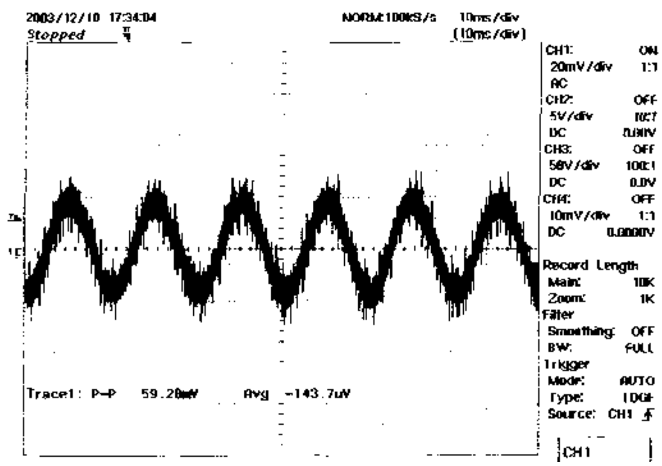

Figure 28 - 48 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{20V}, 20 mV/ div, 1 ms / div

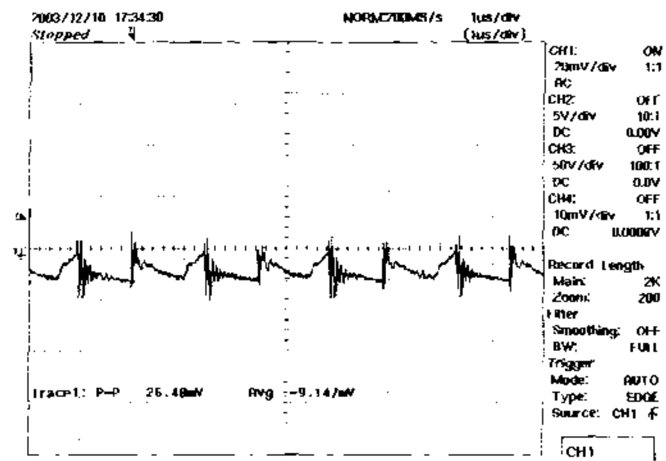

Figure 29 - 48 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{20V}, 20 mV/ div, 1 µs / div

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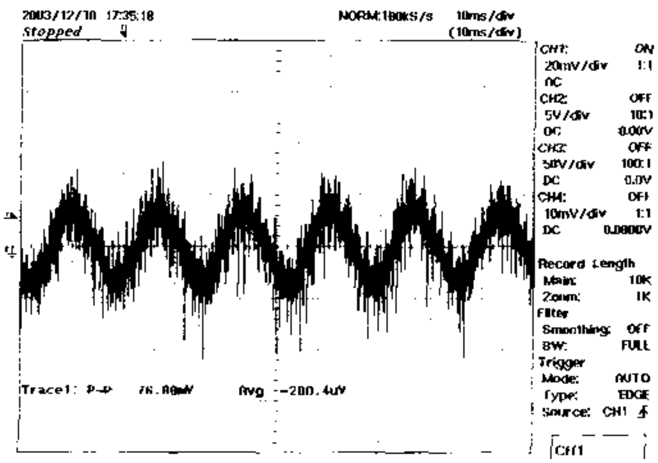

Figure 30 - 72 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{20V}, 20 mV/ div, 1 ms / div

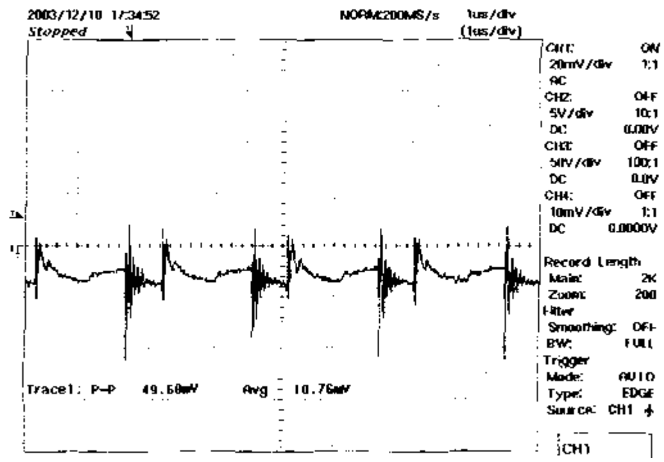

Figure 31 - 72 VDC, Full Load (5 V/2.4 A, 7.5 V/.4 A, 20 V/0.01A)
Upper: V_{20V}, 20 mV/ div, 1 µs / div

11.3 Load Transient Response (50%-75%-50% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

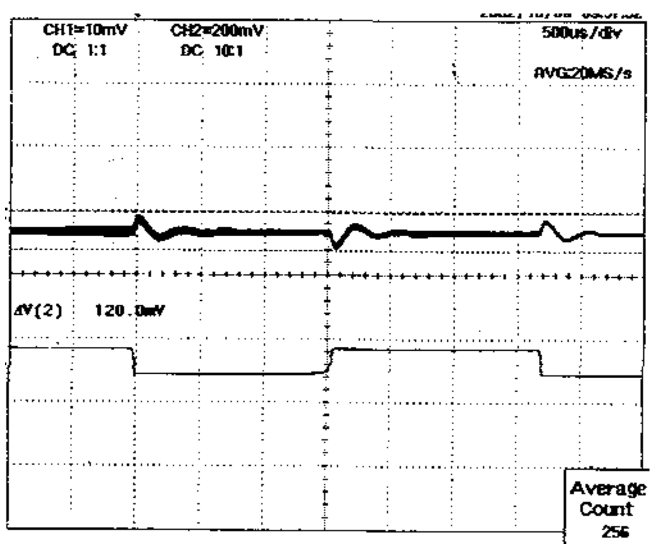

Figure 32 – 36VDC, Output Transient Response. 50-75-50%
Upper: V_{5V}, 10 mV/ div, 500 us / div

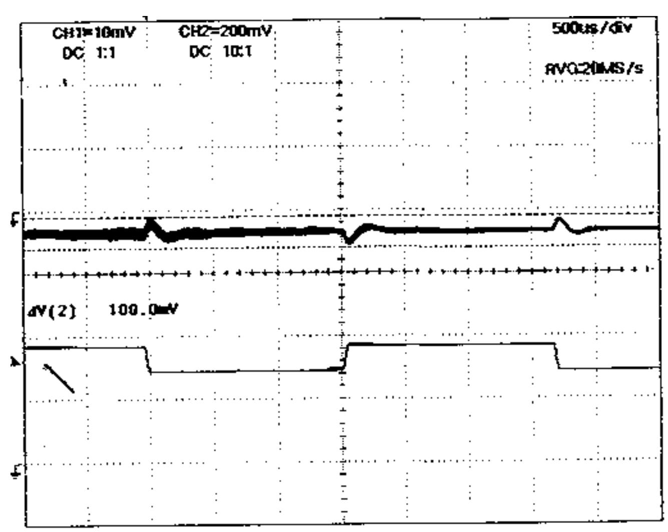

Figure 33 - 72 VDC, Output Transient Response. 50-75-50%
Upper: V_{5V}, 10 mV/ div, 500 us / div

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11.4 Load Transient Response (50%-100%-50% Load Step)

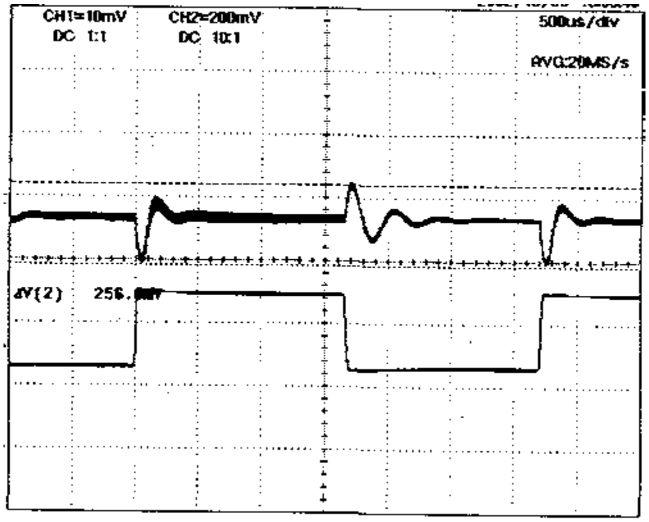

Figure 34 – 36VDC, Output Transient Response. 50-100-50%
Upper: V_{5V}, 10 mV/ div, 500 us / div

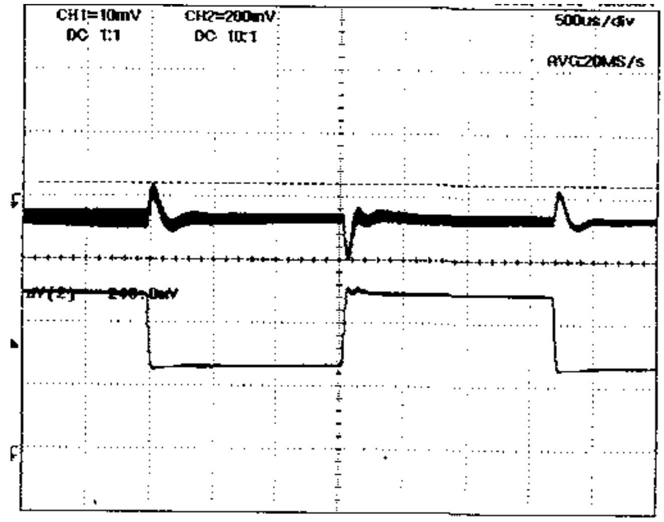

Figure 35 - 72 VDC, Output Transient Response. 50-100-50%
Upper: V_{5V}, 10 mV/ div, 500 us / div

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12 Control Loop Measurements

12.1 36V Maximum Load 25'C

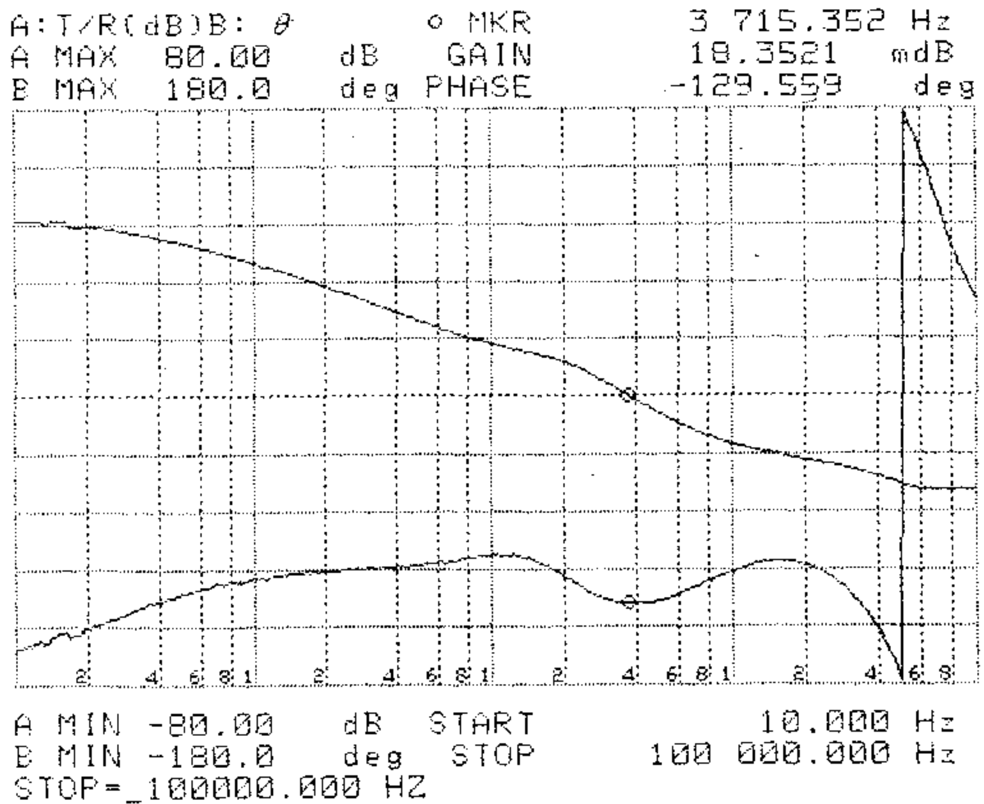

Figure 36 - Gain-Phase Plot, 36 VDC, Full Load Gain Crossover – 3.715 kHz, Phase Margin – 51°

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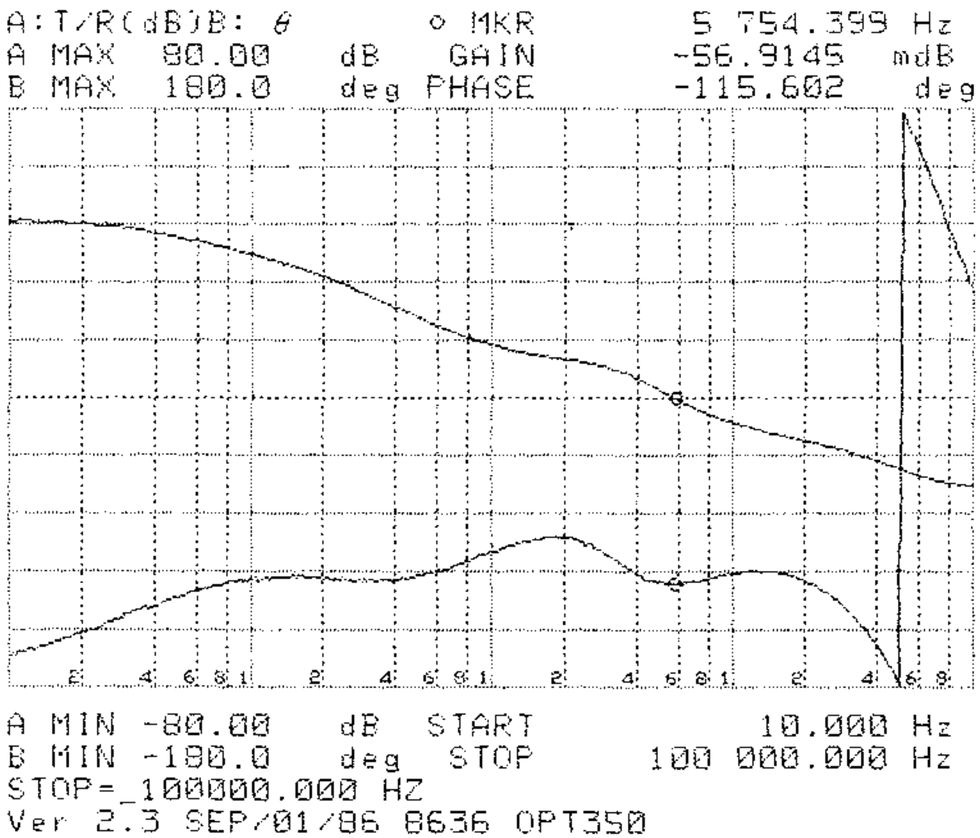

Figure 37 - Gain-Phase Plot, 72 VDC, Full Load Gain Crossover – 5.754 kHz, Phase Margin - 65°

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Revision History

Date	Author	Revision	Description & changes	Reviewed
March 30, 2004	RM/ME	1.0	Initial release	VC / AM

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