Circuit Idea
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An Improved PFC Feedback Loop

Summary of the Idea

An improved feedback loop process is introduced for power factor correction (PFC) controllers in single-stage AC/DC power converters. It reduces external component count and simplifies end-user tuning for the external components of error compensation.

In typical PFC controllers the compensation pin is the output of an operational transconductance amplifier (OTA) externally connected to a resistor and capacitor in parallel (RC). The RC implements a function of proportional (P) plus integral (I), P plus I, on error signal with the resistor and capacitor values determining the proportional gain and integral gain respectively. The proportional term cannot have high gain because it may cause distortion in the input current waveform.

The proposed circuit moves the P gain portion of the feedback loop inside the IC with a higher value fixed P gain that works without causing distortion over a wide range of PFC operating conditions with different values of bulk capacitors. Thus, only the capacitance will remain external and user-adjustable as a means of implementing the slow integrator.

Description

In conventional PFC control methods, a slow voltage feedback loop is required to avoid distortion on the AC input current waveform caused by the 120 Hz ripple on the output bulk capacitor voltage. The relatively slow and low gain creates a challenge for large load transients. The output voltage can dip very low or overshoot to a high value (e.g. <300 V or >450 V for a 380 V set point). The usual solution to this problem is to place a nonlinear amplifier branch or summer (adder) in the feedback loop for when the output voltage goes outside a certain window and to force the controller to respond more quickly to the output voltage dip or overshoot. This approach may have undesirable side effects.

Figure 1 shows a conventional feedback loop inside a PFC controller that uses a P plus I process wherein the feedback signal from the DC output of the converter is applied through the feedback terminal to an error amplifier that is an operational transconductance amplifier OTA, generating the error current signal e(t). The error current signal e(t) is applied to the user selectable external components (R_P and C_{INT}) on the compensation terminal COMP. Resistor R_P introduces the proportional gain $K_P = R_P$ and the value of capacitor C_{INT} introduces integral gain $K_{INT} = 1/C_{INT}$ for the P plus I feedback.

The compensated error signal $K_P e(t) + K_{INT} \int e(t)dt$ is the main power command and would go to the switching modulator.

In contrast to Figure 1, Figure 2 shows the improved PFC control feedback loop using a sample and hold S/H and a proportional, integral and pseudo-derivative (pD) process. The process steps of P plus I plus pD illustrated in Figure 1 are as follows.

In a first step the output voltage or the error of the output voltage is sampled and held (S/H) at every ac zero crossing (or 120 Hz sampling at some specific point on the AC half sinusoid).

The S/H of the error signal is used as the input to the P portion of the error amplifier. Using the S/H version instead of the continuous error signal eliminates waveform distortion due to the 120 Hz ripple on the bulk capacitor. It may then be possible to increase gain for the P process.

The signal from the P process is added to the signal from the I process on the main feedback capacitor on the compensation pin to produce the power command signal for the switching modulator. This closes a P plus I main feedback loop on the amplifier.

The continuous error signal is subtracted from the S/H version of the error signal to produce a pseudo-derivative of the error signal. This method of extracting the derivative due to the time constants involved is easier to implement in an IC compared to an external linear differentiator.

The signal from the pD process with some relative weighting K_{pD} (e.g, $K_{pD} = 2$) is added to the signal from the P process of the continuous error signal to produce a P plus pD (proportional plus pseudo-derivative) control process in the feedback loop. The signal from the P plus pD process is fed into a nonlinear amplifier which has a transfer characteristic with a dead band in the center and steep slopes to the sides, as symbolically illustrated in Figure 2. This is the nonlinear amplifier for addressing large signal transients. During normal operation the nonlinear amplifier is in the dead band region and has no effect on the loop process. The advantage of the signal from a P plus pD process driving the nonlinear amplifier, over a simple error signal, is that the P plus pD process includes information of the rate of change so that it can respond earlier/faster to a rapidly changing output before the error signal may grow too large.

World Headquarters 5245 Hellyer Avenue, San Jose, CA 95138, USA, Main: +1-408-414-9200
Customer Service Phone: +1-408-414-9665, Fax: +1-408-414-9765, Email: info@power.com
On the Web www.power.com

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The nonlinear amplifier, which is an OTA, has a current source output that is fed into the user adjustable external C_{INT} on the compensation terminal that is the main feedback loop integrator.

Therefore, the nonlinear amplifier when operating causes the integrator setting (capacitor voltage) to slew rapidly as needed and prevent large signal overshoots or undershoots.

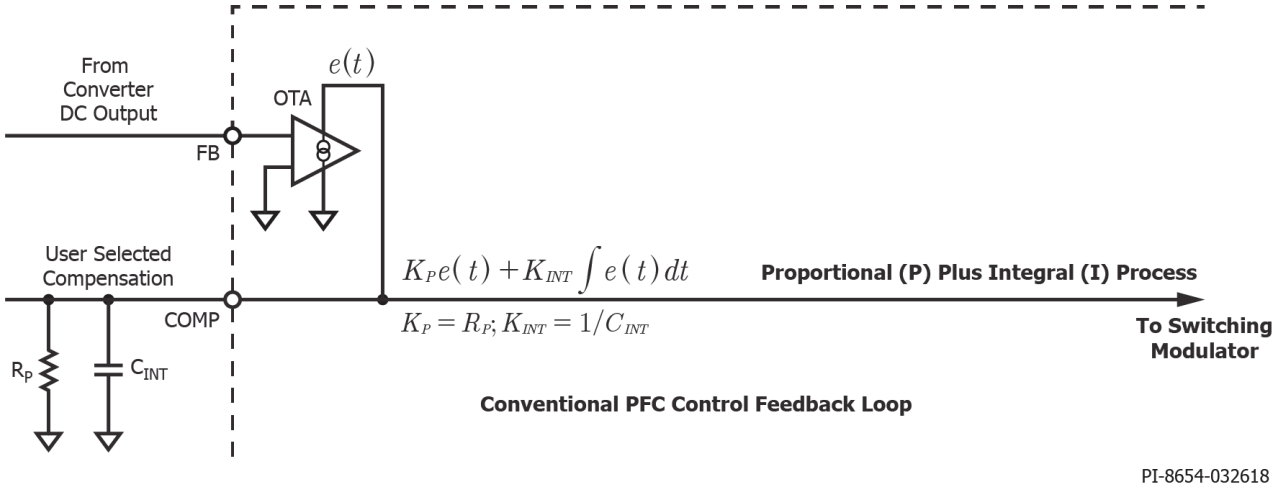

Figure 1. The Conventional PFC Control Feedback Loop with a Simple Proportional (P) Plus Integral (I) Process.

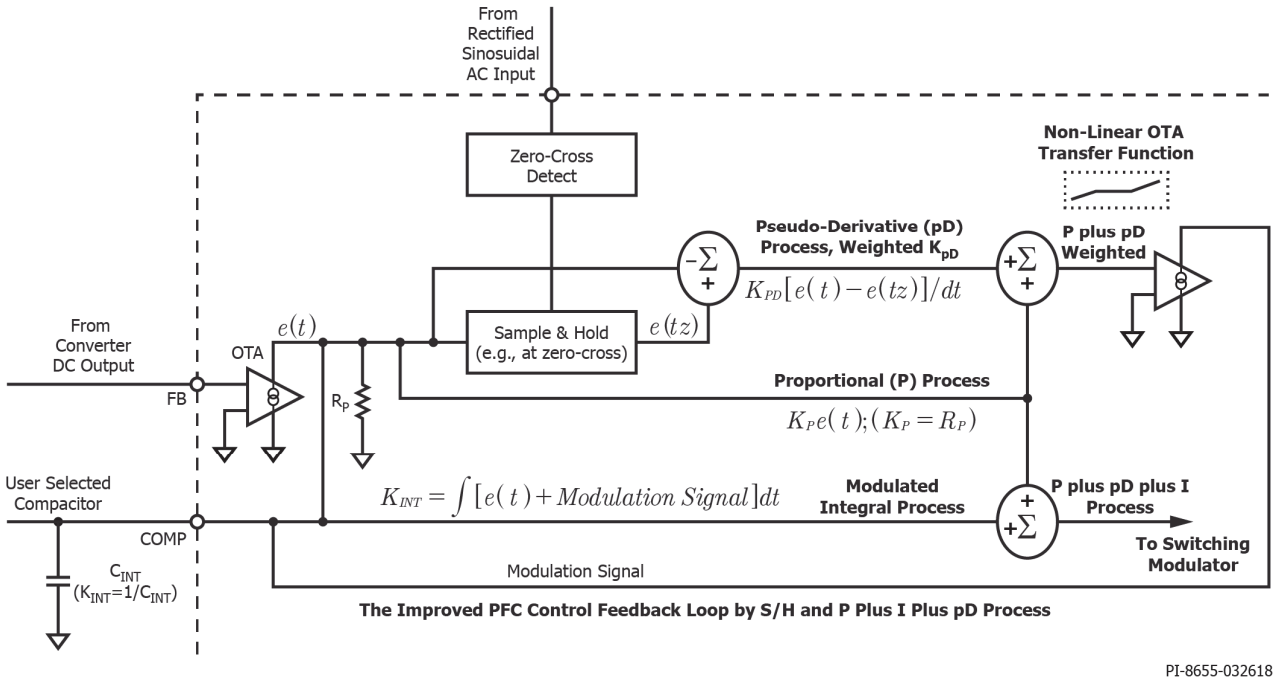

Figure 2: Improved PFC Control Feedback Loop by Using Sample-hold (S/H) and Control Processes Including Proportional (P) plus Integral (I) plus Pseudo-Derivative (pD).

World Headquarters 5245 Hellyer Avenue, San Jose, CA 95138, USA, Main: +1-408-414-9200
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On the Web www.power.com