Circuit Idea
20111202

V Pin Protection Circuit

Summary of the Idea

A controller may use an internal clamp circuit that conducts current from the V pin to prevent damage to the internal ESD (electrostatic discharge) protection structure when the AC input voltage is applied and the supply voltage to the IC is not high enough for the IC to be active. When the IC becomes active, the clamp circuit does not conduct, maintaining high system efficiency.

Description

Figure 1 illustrates a block diagram of a boost converter with the use of a controller that includes an internal ESD protection structure. The ESD protection structure includes a Zener diode VR1 between the INPUT VOLTAGE (V) pin and GROUND (G pin). Figure.1 further illustrates an internal clamp circuit that prevents damage to the ESD protection diode on the V pin when the controller supply voltage VCC is not present.

For the controller in this technical disclosure, the INPUT VOLTAGE (V) pin is used to detect the peak value of the input line voltage directly, receiving a maximum current of 100 μA (limited by resistor R1) from the AC line.

Description (continued)

When the controller is active, internal circuits takes the current from the V pin for control purposes, and the voltage on the V pin is limited to an internal reference voltage of 2.5 volts.

When the controller is not powered up, the internal circuits that would take the current for control purposes are not active. Without a clamp circuit to conduct the current from the AC line, this current can raise the voltage on the V pin high enough to damage the internal ESD protection diode on the V pin. The ESD protection diode conducts when the voltage of the V pin exceeds 9 V. The internal clamp circuit routes the current from the V pin to keep the voltage on the V pin below 9 V.

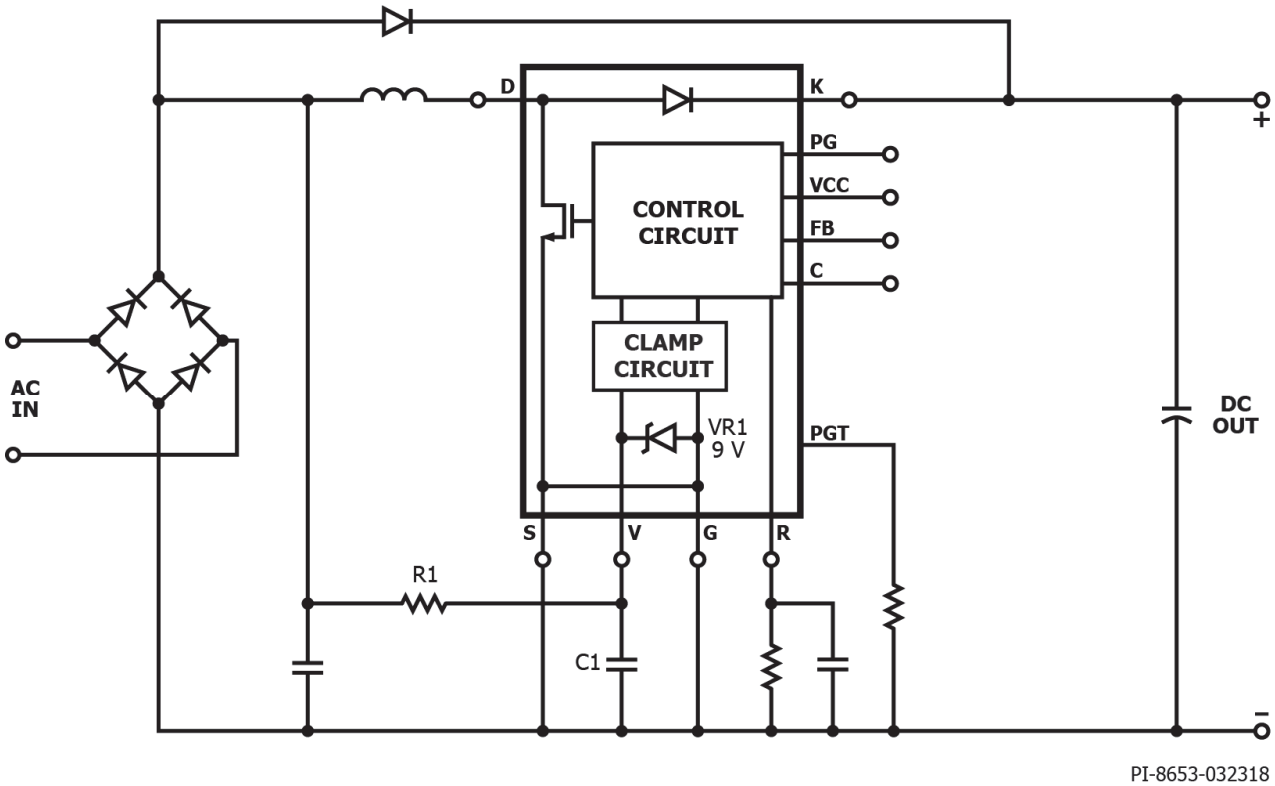

Figure 1. Block Diagram of the Controller with an Internal Clamp Circuit.

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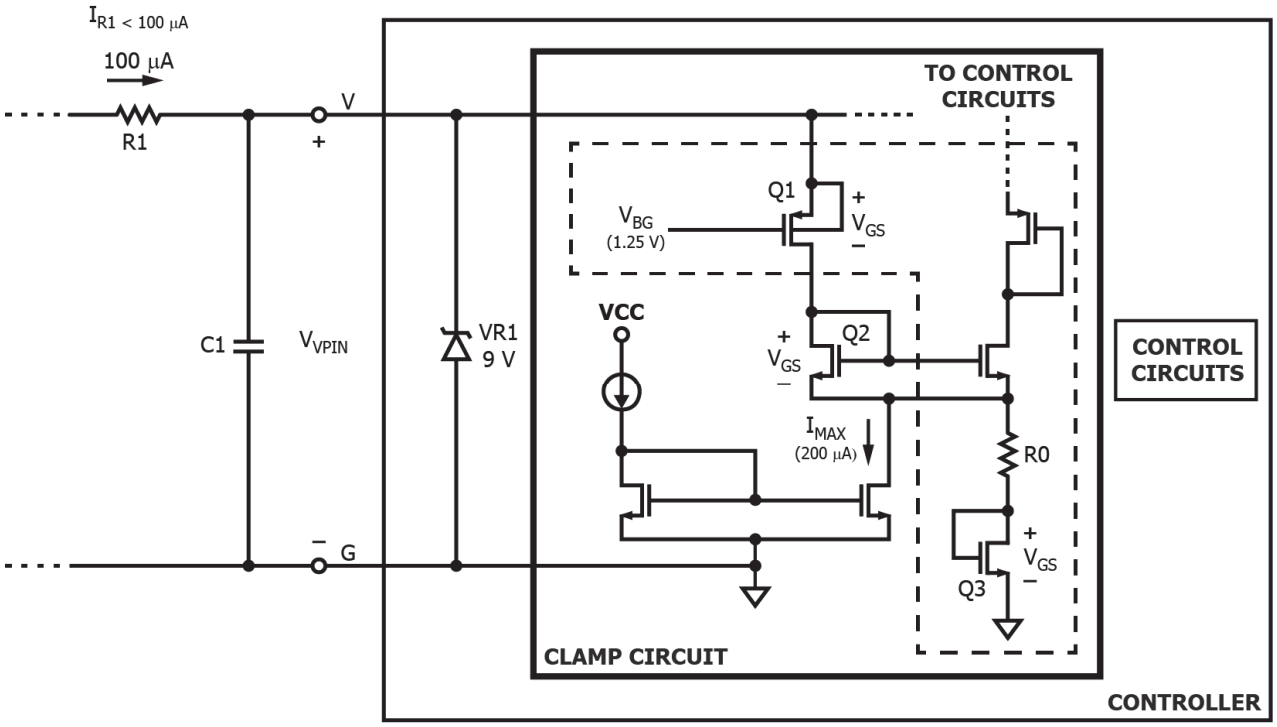

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Figure 2. Clamp Circuit of the Controller.

Description (continued)

Figure 2 illustrates a block diagram of the internal clamp circuit for the controller of this technical disclosure. The clamp circuit is indicated by the dashed box in Figure 2.

The clamp circuit shown in Figure 2 draws enough current from the V pin to keep the voltage below 9 V until the supply voltage VCC is high enough to shut the clamp circuit off. When the supply voltage VCC is low, the bandgap voltage V_{BG} and mirrored current I_{MAX} are approximately zero, and transistors Q1, Q2 and Q3 conduct the all the current entering the V pin.

The voltage of the V pin can be expressed by the equation,

$$V_{VPIN} = I_{R1}R_0 + 3V_{GS}$$

and the voltage on the V pin is limited to less than 9 V.

When the controller supply voltage VCC is greater than 10 V, the bandgap voltage V_{BG} connected to the gate of transistor Q1 is equal to 1.25 V and the mirrored current I_{MAX} sinks currents less than 200 µA. Since the current into the V pin is less than 100 µA, the gate to source voltage of transistor Q3 is reduced to nearly zero volts, and transistor Q3 is turned off. The voltage on V pin is limited to 2.5 V.

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