Application Note AN-70
LinkSwitch-TN2 Family

Design Guide

Introduction

LinkSwitch™-TN2 ICs combine a high-voltage (725 V) power MOSFET switch with an ON/OFF controller onto a monolithic IC. Jitter is added to the switching frequency to achieve lower EMI and the IC is fully fault protected. Auto-restart limits device and circuit dissipation during overload and output short-circuit while over temperature protection disables the internal power MOSFET during thermal faults. The high thermal shutdown threshold is ideal for applications where the ambient temperature is high while the large hysteresis protects the PCB and surrounding components from high average temperatures.

The LinkSwitch-TN2 family is designed for any application where a non-isolated supply is required such as appliances (coffee machines, rice cookers, dishwashers, microwave ovens etc.), night lights, emergency exit signs and LED drivers. LinkSwitch-TN2 ICs can be configured in all common topologies to give a line or neutral referenced output and an inverted or non-inverted output voltage – ideal for applications using TRIACs for AC load control. Using a switching power supply rather than a passive dropper (capacitive or resistive) gives a number of advantages, some of which are listed below.

- Universal input – the same power supply/product can be used worldwide
- High power density – smaller size, typically no X class capacitance needed for most designs
- High efficiency – full load efficiencies >75% typical for 12 V output
- Excellent line and load regulation
- High efficiency at light load – ON/OFF control maintains high efficiency even at light load
- Extremely energy efficient – input power <30 mW at no-load
- Entirely manufacturable with SMD components
- Fully fault protected (overload, short-circuit and thermal faults)
- Scalable – LinkSwitch-TN2 family allows the same basic design to be used from <50 mA to 1000 mA
- Readily available off-the-shelf output inductor

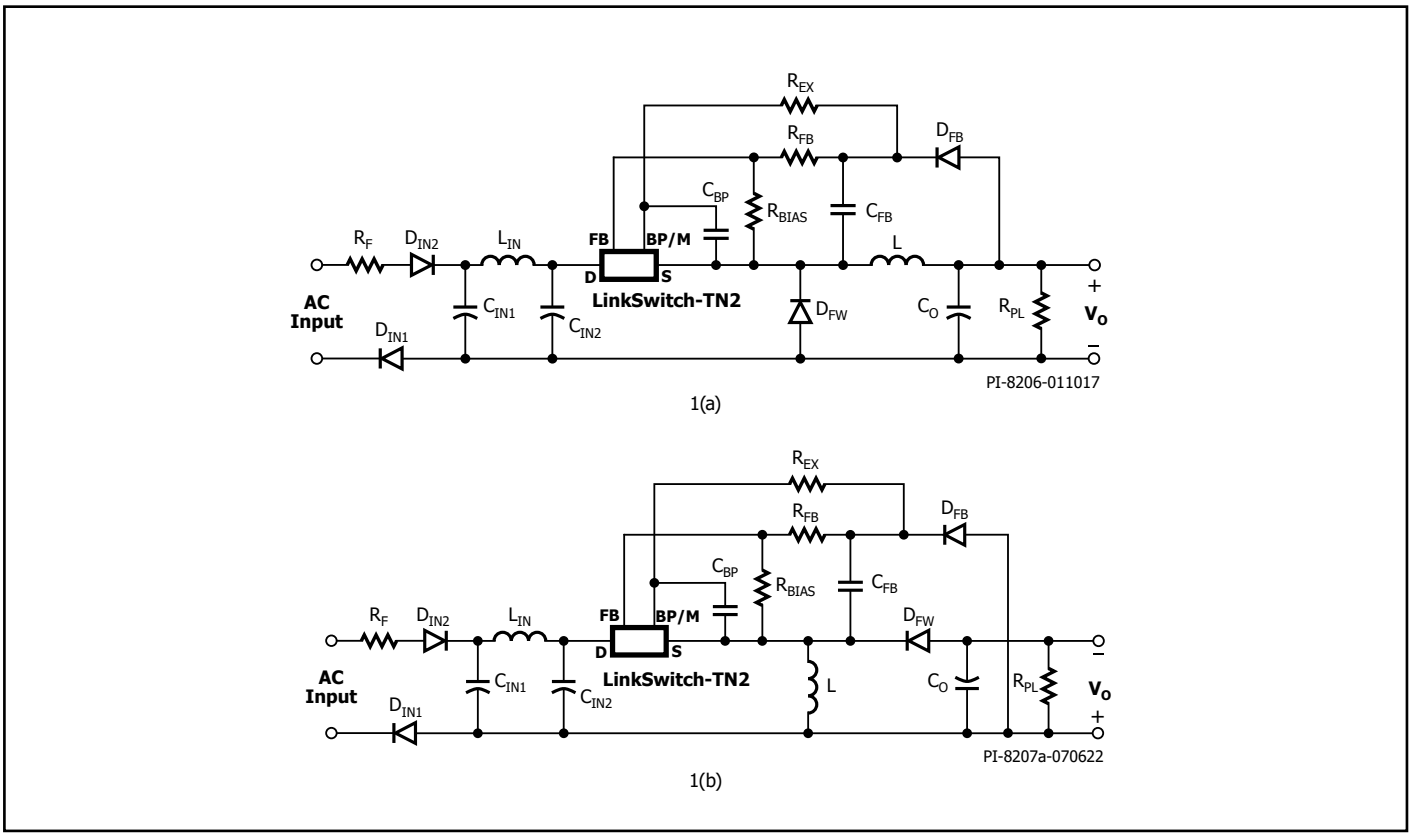


Figure 1. Basic Configuration Using LinkSwitch-TN2 in a Buck Converter, 1(a) and Buck-Boost Converter, 1(b).

Scope

This application note is for designing a non-isolated power supply using the LinkSwitch-TN2 family of devices. This document describes the design procedure for buck and buck-boost converters using the LinkSwitch-TN2 family of integrated off-line switchers. The objective of this document is to provide power supply engineers with guidelines in order to enable them to quickly build efficient and low-cost buck or buck-boost converter based power supplies using low-cost off-the-shelf inductors. Complete design equations are provided for the selection of the converter's key components. Since the power MOSFET and controller are integrated into a single IC, the design process is greatly simplified, the circuit configuration has few parts and no transformer is required. Therefore a quick start section is provided that allows off-the-shelf components to be selected for typical output voltages and currents. To simplify the task this application note refers directly to the PIXIs design spreadsheet that is part of the PI Expert™ design software suite. The basic configuration used in LinkSwitch-TN2 power supplies is shown in Figure 1, which also serves as the reference circuit for component identifications used in the description throughout this application note.

In addition to this application note, the reader may also find the LinkSwitch-TN2 Reference Design Kit (RDK) containing an engineering prototype board, engineering report and device samples useful as an example of a working power supply. Further details on downloading PI Expert, obtaining a RDK and updates to this document can be found at www.power.com.

Quick Start

Readers wanting to start immediately can use the following information to quickly select the components for a new design, using Figure 1 and Tables 1 and 2 as references.

1. For AC input designs select the input stage (Table 10).
2. Select the topology (Tables 1 and 2). If better than ±5% output regulation is required, then use optocoupler feedback with suitable reference such as TL431 or a precision Zener is required.
3. Select the LinkSwitch-TN2 device, L, R_{FB} or V_Z, R_{BIAS}, C_{FB}, R_Z and the reverse recovery time for D_{FW} (Table 4: Buck, Table 5: Buck-Boost).
4. Select freewheeling diode to meet t_{RR} determined in Step 3 (Table 3).
5. For direct feedback designs, if the minimum load <3 mA then calculate $R_{PL} = V_O/3$ mA.
6. Select C_O as 100 µF (LNK3202-6), 220 µF (LNK3207), 330 µF (LNK3208/9). Ensure that the voltage rating is 1.25 × V_O and low ESR type.
7. Construct prototype and verify design.

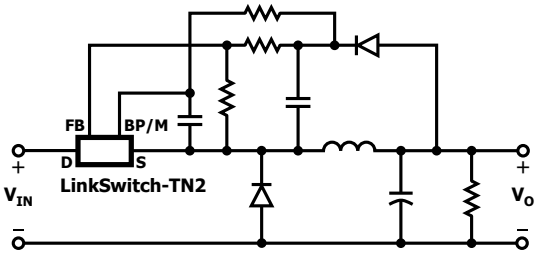
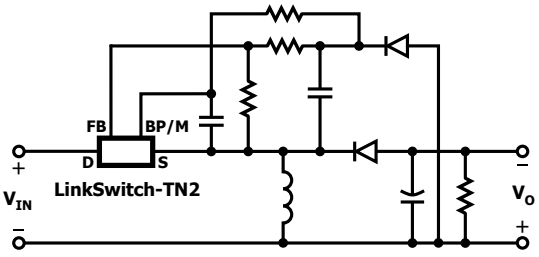
Topology	Basic Circuit Schematic	Key Features
High-Side Buck – Direct Feedback		1. Output referenced to input. 2. Positive output (V_O) with respect to -V_{IN}. 3. Step down : V_O < V_{IN}. 4. Low cost direct feedback (±5% typ.) (Note 1) 5. Requires an output load to maintain regulation (Note 2).
High-Side Buck-Boost – Direct Feedback		1. Output referenced to input. 2. Negative output (V_O) with respect to -V_{IN}. 3. Step down : V_O < V_{IN} (Note 3). 4. Low cost direct feedback (±5% typ.) (Note 1). 5. Fail-safe – output is not subjected to input voltage if the internal MOSFET fails. Ideal for driving LEDs – better accuracy and temperature stability than low-side buck constant current LED driver. 6. Requires an output load to maintain regulation (Note 2).

Table 1. LinkSwitch-TN2 Circuit Configurations using Directly Sensed Feedback.
Notes:
1. Low Cost, directly sensed feedback typically achieves overall regulation tolerance of ±5% with 3 mA pre-load for 12 V design
2. To ensure output regulation, a pre-load may be required to maintain a minimum load current of 3 mA (buck and buck-boost only).
3. Boost topology (step up) is also possible but not shown.

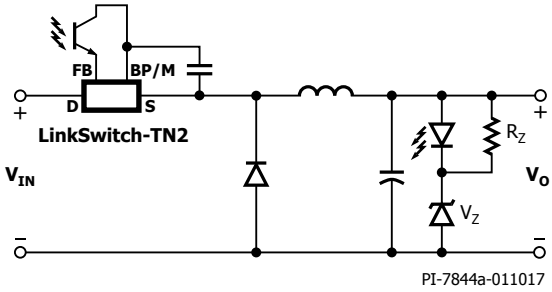
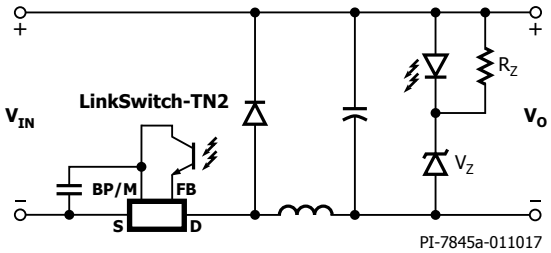
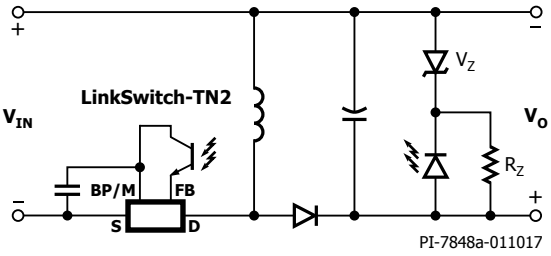
Topology	Basic Circuit Schematic	Key Features
High-Side Buck – Optocoupler Feedback		1. Output referenced to input 2. Positive output (V_O) with respect to $-V_{IN}$ 3. Step down : $V_O < V_{IN}$ 4. Optocoupler feedback - Accuracy only limited by reference choice - Low cost non-safety rated optocoupler - No pre-load required
Low-Side Buck – Optocoupler Feedback		1. Output referenced to input 2. Negative output (V_O) with respect to $+V_{IN}$ 3. Step down : $V_O < V_{IN}$ 4. Optocoupler feedback - Accuracy only limited by reference choice - Low cost non-safety rated optocoupler - No pre-load required
Low-Side Buck-Boost – Optocoupler Feedback		1. Output referenced to input 2. Positive output (V_O) with respect to $+V_{IN}$ 3. Step down : $V_O > V_{IN}$ (Note 3) 4. Optocoupler feedback - Accuracy only limited by reference choice - Low cost non-safety rated optocoupler - No pre-load required 5. Fail-safe – output is not subjected to input voltage if the internal power MOSFET fails

Table 2. LinkSwitch-TN2 Circuit Configurations using Optocoupler Feedback.

Notes:

1. Regulation of optocoupler feedback only limited by accuracy of reference (Zener or IC).
2. Optocoupler does not need to be safety approved.
3. Reference bias current provides minimum load. The value of R_z is determined by Zener test current or reference IC bias current, typically 470 Ω to 2 kΩ, 1/8 W, 5%.
4. Boost topology (step-up) is also possible but not shown.

Part Number	V_{RRM} (V)	I_F (A)	t_{RR} (ns)	Package	Manufacturer
MUR160	600	1	50	Leaded	Vishay
UF4005	600	1	75	Leaded	Vishay
BYV26C	600	1	30	Leaded	Vishay/Philips
STTH1R06	600	1	30	Leaded	ST Microelectronics
STTH1R06A STTH1R06U	600	1	30	SMD	ST Microelectronics
ES1J	600	1	35	SMD	ON Semiconductor
US1J	600	1	75	SMD	Vishay
CD1408-FU1800	800	1	35	SMD	Bourns
STTH3R06U STTH3R06S	600	3	35	SMD	ST Microelectronics

Table 3. List of Ultrafast Diodes Suitable for use as the Freewheeling Diode.

V_{OUT}	$I_{OUT(MAX)}$	Inductor			LNK320X	Mode	Diode t_{RR}	R × FB	V_Z
		μH $I_{RMS(mA)}$	Kemet	Coilcraft					
5	≤63 80	2200 124 2200 84	SBC3-222-191 SBC3-222-191	RFB0807-222L RFB0807-222L	LNK3202	MDCM CCM	≤ 75 ns ≤ 35 ns	3.48 k	3.9 V
	120 170	1000 220 1000 175	SBC4-102-291 SBC4-102-291	RFB0810-102L RFB0810-102L	LNK3204	MDCM CCM	≤ 75 ns ≤ 35 ns		
	175 270	680 320 680 274	SBC4-681-431 SBC4-681-431	RFB0810-681L RFB0810-681L	LNK3205	MDCM CCM	≤ 75 ns ≤ 35 ns		
	225 360	680 465 680 364	–	RFB1010-681L RFB1010-681L	LNK3206	MDCM CCM	≤ 75 ns ≤ 35 ns		
	360 575	470 791 470 581	SBC7-471-851 SBC7-471-851	RFC1010B-474KE RFC1010B-474KE	LNK3207	MDCM CCM	≤ 75 ns ≤ 35 ns		
	485 775	330 1025 330 783	SBC8-331-142 SBC8-331-142	RFS1317-334KL RFS1317-334KL	LNK3208	MDCM CCM	≤ 75 ns ≤ 35 ns		
	600 1000	330 1416 330 1007	SBC8-331-142 SBC8-331-142	RFS1317-334KL RFS1317-334KL	LNK3209	MDCM CCM	≤ 75 ns ≤ 35 ns		
12	≤63 80	2200 87 2400 84	SBC3-222-191 –	RFB0807-222L –	LNK3202	MDCM CCM	≤ 75 ns ≤ 35 ns	11.8 k	11 V
	120 170	1000 155 1600 175	SBC4-102-291 –	RFB0810-102L –	LNK3204	MDCM CCM	≤ 75 ns ≤ 35 ns		
	175 270	680 226 1500 274	SBC4-681-431 –	RFB0810-681L –	LNK3205	MDCM CCM	≤ 75 ns ≤ 35 ns		
	225 360	680 327 1200 364	SBC6-681-631 –	RFB1010-681L RFC1010B-125KE	LNK3206	MDCM CCM	≤ 75 ns ≤ 35 ns		
	360 575	470 558 1000 581	SBC6-471-701 –	RFC1010B-474KE –	LNK3207	MDCM CCM	≤ 75 ns ≤ 35 ns		
	485 775	330 720 560 783	SBC8-331-142 –	RFS1317-334KL RFS1317-564KL	LNK3208	MDCM CCM	≤ 75 ns ≤ 35 ns		
	600 960	330 1001 470 970	SBC8-331-142 –	RFS1317-334KL –	LNK3209	MDCM CCM	≤ 75 ns ≤ 35 ns		
15	≤63 80	2200 80 3300 84	SBC3-222-191 SBC4-332-161	RFB0810-122L RFC1010B-225KE	LNK3202	MDCM CCM	≤ 75 ns ≤ 35 ns	15.4 k	13 V
	120 170	1200 149 2200 175	SBC3-122-281 –	RFB0810-122L RFC1010B-225KE	LNK3204	MDCM CCM	≤ 75 ns ≤ 35 ns		
	175 270	1000 250 1800 274	SBC6-102-561 –	RFC1010B-105KE RFC1010B-185KE	LNK3205	MDCM CCM	≤ 75 ns ≤ 35 ns		
	225 360	680 305 1500 364	SBC6-681-631 SBC6-152-451	RFC1010B-684KE RFC1010B-155KE	LNK3206	MDCM CCM	≤ 75 ns ≤ 35 ns		
	360 575	470 509 1000 581	SBC7-471-851 –	RFC1010B-474KE RFC1010B-105KE	LNK3207	MDCM CCM	≤ 75 ns ≤ 35 ns		
	485 775	330 671 680 783	SBC8-331-142 –	RFS1317-334KL –	LNK3208	MDCM CCM	≤ 75 ns ≤ 35 ns		
	600 960	330 913 560 970	SBC8-331-142 –	RFS1317-334KL –	LNK3209	MDCM CCM	≤ 75 ns ≤ 35 ns		

Other Standard Components
R_{BIAS}: 2.49 kΩ, 1%, 1/8 W
C_{BP}: 0.1 μF, 50 V Ceramic
C_{FB}: 10 μF, 1.25 × V_O
D_{FB}: 1N4005GP
R_Z: 470 Ω to 2 kΩ, 1/8 W, 5%

Table 4. Components Quick Select for Buck Converters. *Select nearest standard or combination of standard values.

V_{OUT}	$I_{OUT(MAX)}$	Inductor			LNK320X	Mode	Diode t_{RR}	R × FB	V_Z
		µH $I_{RMS(mA)}$	Kemet	Coilcraft					
5	≤63 80	1800 70 1800 80	–	RFB0807-182L RFB0807-182L	LNK3202	MDCM CCM	≤ 75 ns ≤ 35 ns	3.44 k	3.9 V
	120 170	820 130 1000 180	–	RFB0807-821L RFB0807-102L	LNK3204	MDCM CCM	≤ 75 ns ≤ 35 ns		
	175 270	680 200 820 270	–	RFB0810-681L RFB0810-821L	LNK3205	MDCM CCM	≤ 75 ns ≤ 35 ns		
	225 360	680 250 680 370	SBC4-681-431 SBC4-681-431	RFB0810-681L RFB0810-681L	LNK3206	MDCM CCM	≤ 75 ns ≤ 35 ns		
	360 575	470 410 470 590	SBC6-471-701 SBC6-471-701	RFB1010-471L RFB1010-471L	LNK3207	MDCM CCM	≤ 75 ns ≤ 35 ns		
	485 775	470 540 470 790	SBC8-471-112 SBC8-471-112	RFS1317-474KL RFS1317-474KL	LNK3208	MDCM CCM	≤ 75 ns ≤ 35 ns		
	600 1000	470 670 470 1020	–	MSS1583-474 MSS1583-474	LNK3209	MDCM CCM			
12	≤63 80	2700 80 3300 90	– SBC4-332-161	RFB0807-272L RFB0807-332L	LNK3202	MDCM CCM	≤ 75 ns ≤ 35 ns	11.45 k	11 V
	120 170	1200 150 2200 190	– SBC6-222-351	RFB1010-122L RFB0807-222L	LNK3204	MDCM CCM	≤ 75 ns ≤ 35 ns		
	175 270	820 220 1800 300	–	RFB0810-821L RFB1010-182L	LNK3205	MDCM CCM	≤ 75 ns ≤ 35 ns		
	225 360	680 280 1800 400	SBC6-681-631 –	RFB0810-681L –	LNK3206	MDCM CCM	≤ 75 ns ≤ 35 ns		
	360 575	470 450 1000 640	SBC6-471-701 –	RFB1010-471L –	LNK3207	MDCM CCM	≤ 75 ns ≤ 35 ns		
	485 775	470 600 820 860	SBC8-471-112 –	RFS1317-474KL –	LNK3208	MDCM CCM	≤ 75 ns ≤ 35 ns		
	600 960	470 730 680 1100	–	MSS1583-474 –	LNK3209	MDCM CCM	≤ 75 ns ≤ 35 ns		
15	≤63 80	3300 80 3900 90	SBC4-332-161 –	RFB0810-332L RFB0810-392L	LNK3202	MDCM CCM	≤ 75 ns ≤ 35 ns	14.89 k	13 V
	120 170	1500 150 2700 200	SBC4-152-221 –	RFB0810-152L RFB1010-272L	LNK3204	MDCM CCM	≤ 75 ns ≤ 35 ns		
	175 270	1000 220 2200 310	SBC6-102-561 SBC6-222-351	RFB0810-102L RFB1010-222L	LNK3205	MDCM CCM	≤ 75 ns ≤ 35 ns		
	225 340	820 280 1800 380	–	RFB1010-821L –	LNK3206	MDCM CCM	≤ 75 ns ≤ 35 ns		
	360 575	560 460 1200 660	–	RFS1317-564KL –	LNK3207	MDCM CCM	≤ 75 ns ≤ 35 ns		

Other Standard Components
R_{BIAS}: 2.49 kΩ, 1%, 1/8 W
C_{BP}: 0.1 µF, 50 V Ceramic
C_{FB}: 10 µF, 1.25 × V_O
D_{FB}: 1N4005GP
R_Z: 470 Ω to 2 kΩ, 1/8 W, 5%

Table 5. Components Quick Select for Buck-Boost Converters. *Select nearest standard or combination of standard values. The inductor values indicated in the table above are conservative estimates. In some designs it may be possible to reduce the inductance value further based on evaluation results.

LinkSwitch-TN2 Circuit Design

LinkSwitch-TN2 Operation

The basic circuit configuration for a buck converter using a LinkSwitch-TN2 IC is shown in Figure 1(a). To regulate the output, an ON/OFF control scheme is used as illustrated in Table 6. As the decision to switch is made on a cycle-by-cycle basis, the resultant power supply has extremely good transient response and removes the need for control loop compensation components. If no feedback is received for 50 ms, then the supply enters auto-restart mode of operation and switching is inhibited for a period of time to limit power dissipation.

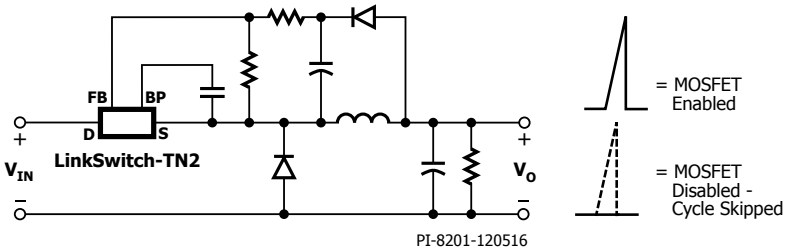
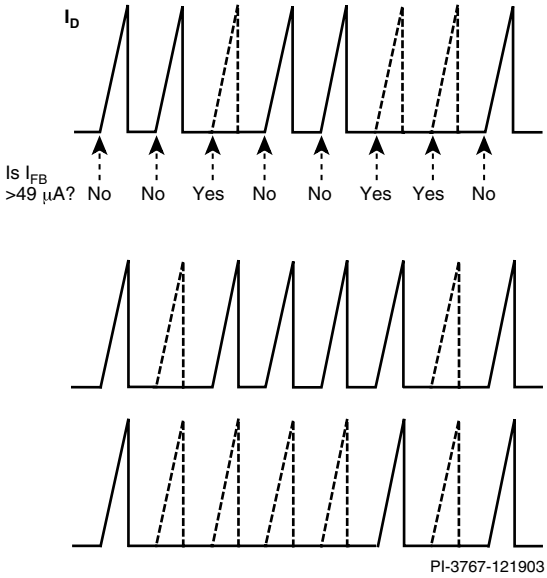
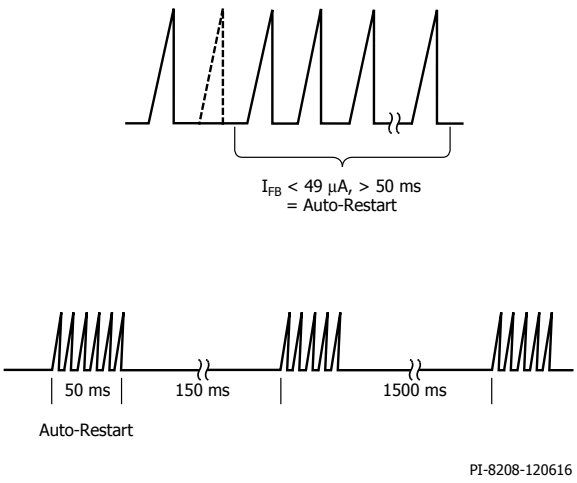
Reference Schematic And Key		
Normal Operation		At the beginning of each cycle, the FEEDBACK (FB) pin is sampled. • If I_{FB} < 49 µA then next cycle occurs • If I_{FB} > 49 µA then next switching cycle is skipped High load – few cycles skipped Low load – many cycles skipped
Auto-Restart		If no feedback (I_{FB} < 49 µA) for > $t_{AR(ON)}$ (50 ms), then output switching is disabled equal to the auto-restart off-time. The first time a fault is asserted the off-time is 150 ms ($t_{AR(OFF)}$ first off period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ subsequent periods).

Table 6. LinkSwitch-TN2 Operation.

To allow direct sensing of the output voltage without the need for a reference (Zener diode or reference IC), the FEEDBACK pin voltage is tightly toleranced over the entire operating temperature range. For example, this allows a 12 V design with an overall output tolerance of ±5%. For higher performance, an optocoupler can be used with a reference as shown in Table 2. Since the optocoupler just provides level shifting, it does not need to be safety rated or approved. The use of an optocoupler also allows flexibility in the location of the device, for example it allows a buck converter configuration with the LinkSwitch-TN2 IC in the low-side return rail, reducing EMI as the SOURCE pins and connected components are no longer part of the switching node.

Selecting the Topology

If possible, use the buck topology. The buck topology maximizes the available output power from a given LinkSwitch-TN2 IC and inductor value. Also, the voltage stress on the power switch and freewheeling diode and the average current through the output inductor are slightly lower in the buck topology as compared to the buck-boost topology.

Selecting the Operating Mode – MDCM and CCM Operation

At the start of a design, select between mostly discontinuous conduction mode (MDCM) and continuous conduction mode (CCM) as this decides the selection of the LinkSwitch-TN2 device, freewheeling diode and inductor. For maximum output current select CCM, for all other cases MDCM is recommended. Overall, select the operating mode and components to give the lowest overall solution cost. Table 7 summarizes the trade-offs between the two operating modes.

Additional differences between CCM and MDCM include better transient response for DCM and lower output ripple (for same capacitor ESR) for CCM. However these differences, at the low output currents of LinkSwitch-TN2 applications, are normally not significant.

The conduction mode CCM or MDCM of a buck or buck-boost converter primarily depends on input voltage, output voltage, output current and device current limit. The input voltage, output voltage and output current are fixed design parameter; therefore the LinkSwitch-TN2 current limit is the only design parameter that sets the conduction mode.

The phrase "mostly discontinuous" is used as with On/Off control, since a few switching cycles may exhibit continuous inductor current, the majority of the switching cycles will be in the discontinuous conduction mode. A design can be made fully discontinuous but that will limit the available output current, making the design less cost effective.

Comparison of CCM and MDCM Operating Modes

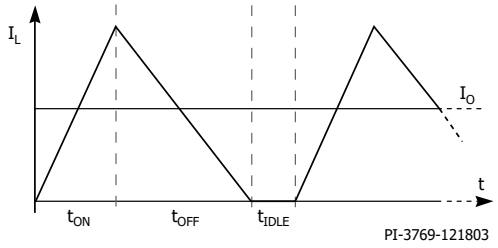
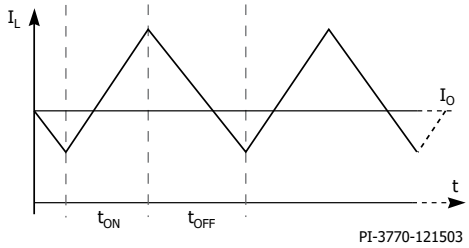
Operating Mode	MDCM	CCM
Operating Description	 Inductor current falls to zero during t_{OFF}, boarder-line between MDCM and CCM when t_{IDLE} = 0.	 Current flows continuously in the inductor for the entire duration of a switching cycle.
Inductor	**Lower Cost** Lower value, smaller size.	**Higher Cost** Higher value, larger size.
Freewheeling Diode	**Lower Cost** 75 ns ultrafast reverse recovery type (≤35 ns for ambient >70 °C).	**Higher Cost** 35 ns ultrafast recovery type required.
LinkSwitch-TN2	**Potentially Higher IC Cost** May require larger device to deliver required output current – depends on required output current.	**Potentially Lowest IC Cost** May allow smaller device to deliver required output current, depends on required output current.
Efficiency	**Higher Efficiency** Lower switching losses.	**Lower Efficiency** Higher switching losses.
Overall	Typically lower cost but reduced output power	Typically higher cost but increased output power

Table 7. Comparison of Mostly Discontinuous Conduction (MDCM) and Continuous Conduction (CCM) Modes of Operation.

ON/OFF Operation with Current Limit State Machine

LNK3207/8/9 has a special operating mode in which the current limit has multiple states depending on the output load. It has an advantage of generating less audible noise across varying load.

The internal clock of the LNK3207/8/9 runs all the time. At the beginning of each clock cycle, it samples the FEEDBACK pin to decide whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine reduces the current limit to reduced values.

At near maximum load, LNK3207/8/9 will conduct during nearly all of its clock cycles (Figure 2). At slightly lower load, it will "skip" additional cycles in order to maintain voltage regulation at the power supply output (Figure 3). At medium loads, cycles will be skipped and the current limit will be reduced (Figure 4). At very light loads, the current limit will be needed to reduced even further (Figure 5). Only a small percentage of cycles will be needed to occur to satisfy the power consumption of the power supply.

The response time of the ON/OFF control scheme is very fast compared to PWM control. This provides accurate regulation and excellent transient response.

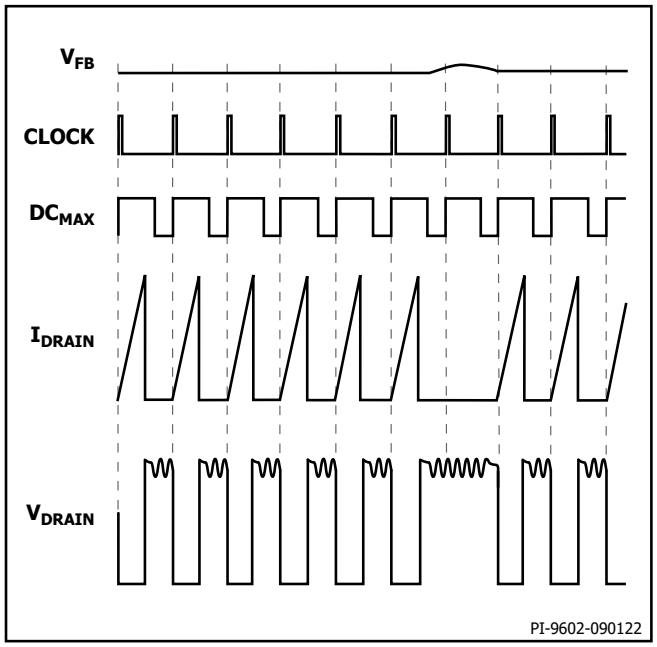


Figure 2. Operation at Near Maximum Loading (Buck).

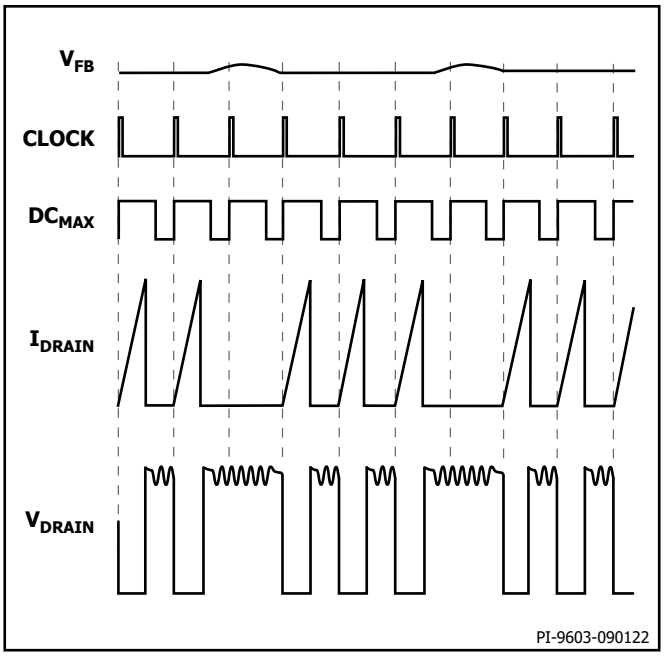


Figure 3. Operation at Moderately Heavy Loading (Buck).

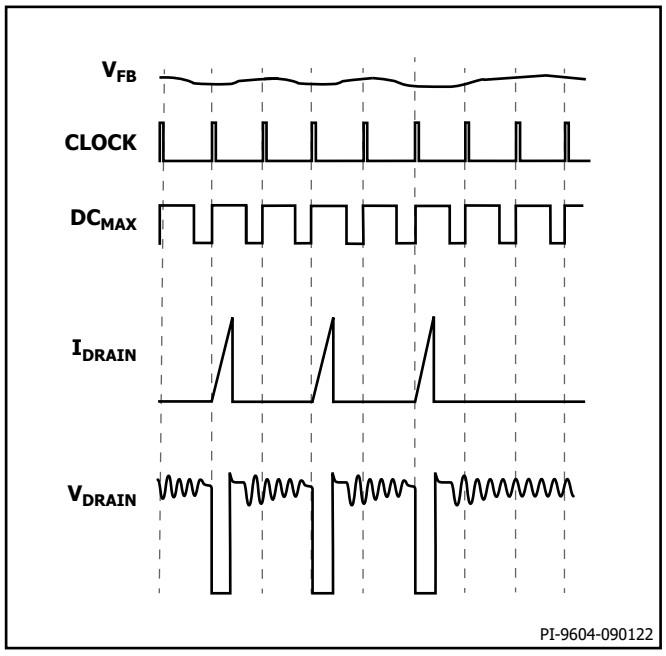


Figure 4. Operation at Medium Loading (Buck).

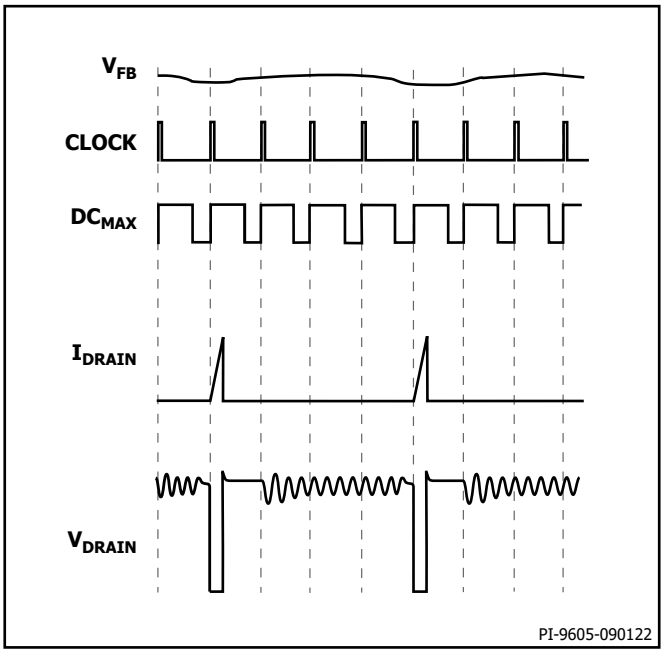


Figure 5. Operation at Very Light Load (Buck).

Step-by-Step Design Procedure

Step 1 – Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, I_O, η, C_{IN}

ENTER APPLICATION VARIABLES				
LINE VOLTAGE RANGE		Universal		AC line voltage range
VACMIN	**85.00**	85.00	volts AC	Minimum AC line voltage
VACTYP		115.00	volts AC	Typical AC line voltage
VACMAX	**265.00**	265.00	volts AC	Maximum AC line voltage
fL		50.00	Hz	AC mains frequency
LINE RECTIFICATION TYPE	**H**	H		Select 'F'ull wave rectification or 'H'alf wave rectification
t_CONDUCTION		2.72	ms	Enter the bridge diode conduction time
VOUT	**12.00**	12.00	volts DC	Output voltage
IOUT	**0.120**	0.120	A	Average output current
EFFICIENCY_ESTIMATED		0.75		Efficiency estimate at output terminals
EFFICIENCY_CALCULATED		0.82		Calculated efficiency based on real components and operating point
POUT		1.44	W	Continuous Output Power
CIN	**9.40**	9.40	uF	Input capacitor
VMIN		86.0	volts DC	Valley of the rectified input voltage
VMAX		374.8	volts DC	Peak of the rectified maximum input AC voltage
T_AMBIENT		50	degC	Operating ambient temperature in degrees celcius
INPUT STAGE RESISTANCE		10	mohms	Input stage resistance in milliohms (includes fuse, thermistor, filtering components)
PLOSS_INPUTSTAGE		0.000	W	Input stage losses estimate

Figure 6. Application Variable Section of LinkSwitch-TN2 Design Spreadsheet.

Input Voltage
Determine the input voltage range from Table 8.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100/115	85	132
230	195	265
Universal	85	265

Table 8. Standard Worldwide Input Line Voltage Ranges.

Line Frequency, f_L
50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimum. For most applications this gives adequate overall design margin. For absolute worst case or based on the product specification reduce these numbers by 6% (47 Hz or 56 Hz).

Nominal Output Voltage, V_{OUT} (V)
Enter the nominal output voltage of the main output during the continuous load condition. Generally the main output is the output from which feedback is derived.

Output Current, I_{OUT} (A)
Enter the output current of the power supply. This is the maximum allowable continuous load of the power supply.

Power Supply Efficiency, η
Enter the estimated efficiency of the complete power supply measured at the output terminals under peak load conditions and worst-case line (generally lowest input voltage). Start with a value of 0.7 for a 12 V output, 0.55 for a 5 V output if no better reference data available, typical for a design where the majority of the output power is drawn from an output voltage of 12 V or greater. Once a prototype has been constructed then the measured efficiency should be entered.

Total Input Capacitance, C_{IN} (μF)
Enter total input capacitance using Table 9 for guidance.

The capacitance is used to calculate the minimum and maximum rectified input AC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage, V_{MIN} > 70 V.

	Minimum Total Input Capacitance per Watt Output Power μF/W	
AC Input Voltage (VAC)	Full-Wave Rectification	Half-Wave Rectification
100/115	2	4-5
230	1	1-2
85-265	2	4-5

Table 9. Suggested Total Input Capacitance Values for Different Input Voltage Ranges.

Step 2 – Determine AC Input Stage

The input stage comprises fusible resistor(s), input rectification diodes and line filter network. Flameproof fusible resistors are recommended to be chosen and depending on the differential line input surge requirements, a wire-wound type may be required. The fusible resistor(s) provides fuse safety, inrush current limiting and differential mode noise attenuation. For increase efficiency at output power > 1 W, fusible resistor can be replaced with a fuse. The EMI performance of half-wave rectified designs is improved by adding a second diode in the lower return rail. This provides EMI gating (EMI currents only flow when the diode is conducting) and also doubles differential surge withstand as the surge voltage is shared across two diodes. Table 10 shows the recommended input stage based on output power for a universal input design while Table 9 shows how to adjust the input capacitance for other input voltage ranges.

Step 3 – Determine Minimum and Maximum DC Input Voltages V_{MIN} and V_{MAX} Based on AC Input Voltage

Calculate V_{MAX} as:

$$V_{MAX} = \sqrt{2} \times V_{ACMAX} \quad (1)$$

Assuming that the value of input fusible resistor is small, the voltage drop across it can be ignored.

Derive minimum input voltage V_{MIN}.

Half bridge rectifier:

$$V_{MIN} = \sqrt{(2 \times V_{ACMIN}{}^2) - \frac{2 \times P_O\left(\frac{1}{2 \times f_L} - t_C\right)}{\eta \times C_{IN(TOTAL)}}} \quad (2)$$

Full bridge rectifier:

$$V_{MIN} = \sqrt{(2 \times V_{ACMIN}{}^2) - \frac{2 \times P_O\left(\frac{1}{2 \times f_L} - t_C\right)}{\eta \times C_{IN(TOTAL)}}} \quad (3)$$

If V_{MIN} is ≤ 70 V then increase value of $C_{IN(TOTAL)}$. t_C is the bridge diode conduction time.

Step 4 – Select LinkSwitch-TN2 Device Based on Output Current and Current Limit

Decide on the operating mode – refer to Table 7.

For MDCM operation, the output current (I_O) should be less than or equal to half the value of the minimum current limit of the chosen device from the data sheet.

$$I_{LIMIT\_MIN} > 2 \times I_O \quad (4)$$

For CCM operation, the device should be chosen such that the output current I_O, is more than 50%, but less than 80% of the minimum current limit I_{LIMIT_MIN}.

$$0.5 \times I_{LIMIT\_MIN} < I_O < 0.8 \times I_{LIMIT\_MIN} \quad (5)$$

Please see the data sheet for LinkSwitch-TN2 current limit values.

A typical LinkSwitch-TN2 part can be programmed to operate in one of the two current limits. The "RED" or reduced current limit enables operation at a reduced current limit and is recommended when the part is to be used at a current level considerably lower than the rated output current. A "STD" or standard current limit will be selected in most applications to optimize on BP capacitor cost.

Use of a 0.1 µF capacitor results in the standard current limit value. Use of a 1 µF capacitor results in the current limit being reduced, allowing design with lowest cost buck chokes.

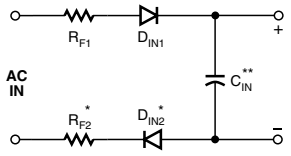
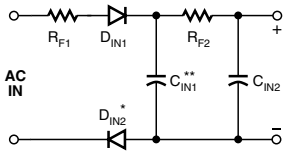
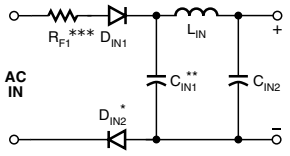
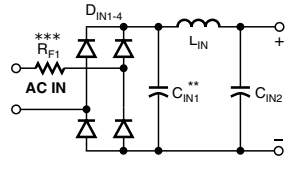
POUT	≤0.25 W	0.25 - 1 W	>1 W	
85 - 265 VAC Input Stage	 PI-3771-121603	 PI-3772-121603	 PI-3773-121603	 PI-3774-121603
	R_{F1}, R_{F2}: 100-470 Ω, 0.5 W, Fusible C_{IN}: ≥2.2 µF, 400 V D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 Ω, 1 W Fusible R_{F2}: 100 Ω, 0.5 W, Flameproof C_{IN1}, C_{IN2}: ≥3.3 µF, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 Ω, 1 W Fusible L_{IN}: 470 µH – 2.2 mH, 0.05 A – 0.3 A C_{IN1}, C_{IN2}: ≥4 µF/W_{OUT}, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V	R_{F1}: 8.2 Ω, 1 W Fusible L_{IN}: 470 µH – 2.2 mH, 0.05 A – 0.3 A C_{IN1}, C_{IN2}: ≥2 µF/W_{OUT}, 400 V each D_{IN1}, D_{IN2}: 1N4007, 1 A, 1000 V
Comments	*Optional for improved EMI and line surge performance. Remove for designs requiring no impedance in return rail. **Increase value to meet required differential line surge performance. ***Can be replaced by a fuse to increase efficiency.			

Table 10. Recommended AC Input Stages for Universal Input.

Step 5 – Select the Output Inductor

Choose any standard off-the-shelf inductor that meets the design requirements. As shown in the figure below, a "drum" or "dog bone" "I" core inductor is recommended with a single ferrite element due to its low cost and very low audible noise properties. However, the inductor should be selected as varnished type in order to get low audible noise.

Tables 4 and 5 provide inductor values and RMS current ratings for common output voltages and currents based on the calculations in the design spreadsheet. Select the next nearest higher voltage and/or current above the required output specification. Alternatively, the PIXls spreadsheet tool in the PI Expert software design suite or Appendix B can be used to calculate the exact inductor value (Eq. C13) and RMS current rating (Eq. C29). It is recommended that the value of inductor chosen should be closer to L_{TYP} rather than 1.5 × L_{TYP} due to lower DC resistance and higher RMS rating. The lower limit of 330 µH limits the maximum di/dt to prevent very high peak current values.

$$330\ \mu H < L < 1.5 \times L_{TYP}$$

For LinkSwitch-TN2 designs, the mode of operation is not dependent on the inductor value. The mode of operation is a function of load current and current limit of the chosen device. The inductor value merely sets the average switching frequency. Figure 8 shows a typical standard inductor manufacturer's data sheet. The value of off-the-shelf "drum core / dog bone / I core" inductors will drop up to 20% in value as the current increases. The constant K_{L_TOL} in equation (C14) and the design spreadsheet adjusts for both this drop and the initial inductance value tolerance. For example if a 680 µH, 360 mA inductor is required, referring to Figure 8, the tolerance is 10% and an estimated 9.5% for the reduction in inductance at the operating current (approximately [0.36/0.38] × 10). Therefore the value of K_{L_TOL} = 0.195 (19.5%). If no data is available, assume a K_{L_TOL} of 0.15 (15%).

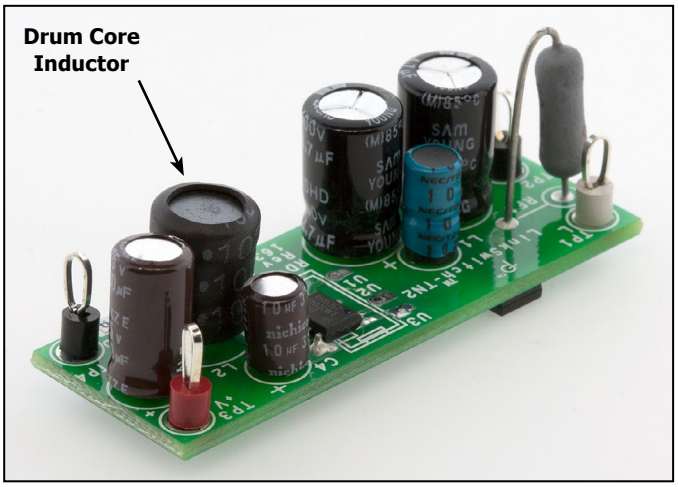


Figure 7. Example of the Drum Core Inductor.

Not all the energy stored in the inductor is delivered to the load, due to losses after the LinkSwitch-TN2 device, the inductor (resistance of winding and core losses), the freewheeling diode, feedback circuit, output capacitor loss and preload. This will limit the maximum power delivering capability and thus reduce the maximum output current. The minimum inductance must compensate for these losses in order to deliver specified full load power. To compensate for this, a loss factor K_{LOSS} is used. This has a recommended value of between 50% and 66% of the total supply losses as given by Equation 6. For example, a design with an overall efficiency (η) of 0.75 would have a K_{LOSS} value of between 0.875 and 0.833.

$$K_{LOSS} = 1 - \left(\frac{1-\eta}{2}\right) to\ 1 - \left(\frac{2(1-\eta)}{3}\right) \quad (6)$$

● SBC3 Series

Model	Inductance L(mH) at 10 kHz)	Rdc (Ω) max.	Rated Current (A) ΔT = 20 °C	Current (Reference Value) (A) ΔT = 40 °C	Current (Reference Value) (A) L change rate -10%
681-361	680±10%	1.62	0.36	0.50	0.38
102-281	1000±10%	2.37	0.28	0.39	0.31
152-251	1500±10%	3.64	0.25	0.35	0.26
222-191	2200±10%	5.62	0.19	0.26	0.21
332-151	3300±10%	7.66	0.15	0.21	0.17

Inductance and Tolerance
Current Rating for 20 °C Rise
Current Rating for 40 °C Rise
Current Rating for Value -10%

PI-3783-030217

Figure 8. Example of Standard Inductor Data Sheet.

Step 6 – Select Freewheeling Diode

For MDCM operation at t_{AMB} ≤ 70 °C, select an ultrafast diode with t_{RR} ≤ 75 ns. At t_{AMB} > 70 °C, t_{RR} ≤ 35 ns. For CCM operation, select an ultrafast diode with t_{RR} ≤ 35 ns. Allowing 25% design margin for the freewheeling diode,

$$V_{PIV} > 1.25 \times V_{MAX} \quad (7)$$

The diode must be able to conduct the full load current. Thus:

$$I_F > 1.25 \times I_O \quad (8)$$

Table 3 lists common freewheeling diode choices.

Step 7 – Select Output Capacitor

The output capacitor should be chosen based on the output voltage ripple requirement. Typically the output voltage ripple is dominated by the capacitor ESR and can be estimated as:

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (9)$$

where V_{RIPPLE} is the maximum output ripple specification and I_{Ripple} is the LinkSwitch-TN2 output ripple current (Refer to C2 and C3).

The capacitor ESR value should be specified approximately at the switching frequency of 66 kHz. Capacitor values above 100 µF for LNK3202-6, 220 µF for LNK3207, and 330 µF for LNK3208/9 are not recommended as they can prevent the output voltage from reaching regulation during the 50 ms period prior to auto-restart. If more capacitance is required, then a soft-start capacitor should be added (see Tips for Designs section) or use larger device of LinkSwitch-TN2. Select a voltage rating such that V_{RATED} ≥1.25 × V_O.

Step 8 – Select the Feedback Resistors

The values of R_{FB} and R_{BIAS} are selected such that, at the regulated output voltage, the voltage on the FEEDBACK pin (V_{FB}) is 2 V. This voltage is specified for a FEEDBACK pin current (I_{FB}) of 49 µA.

Let the value of R_{BIAS} = 2.49 kΩ; this biases the feedback network at a current of ~0.8 mA. Hence the value of R_{FB} is given by:

$$R_{FB} = \frac{V_O - V_{FB}}{\frac{V_{FB}}{R_{BIAS}} + I_{FB}} = \frac{(V_O - V_{FB}) \times R_{BIAS}}{V_{FB} + (I_{FB} \times R_{BIAS})} \quad (10)$$

Step 9 – Select the Feedback Diode and Capacitor

For the feedback capacitor, use a 10 µF general purpose electrolytic capacitor with a voltage rating ≥1.25 × V_O. For the feedback diode, use either low cost glass passivated diode (1N4005GP or DFLR1600-7) or ultrafast diode (BYV26C or STTH1R06) with a voltage rating of ≥1.25 x V_{MAX}. Ultrafast diode speed up the feedback capacitor charging at start-up that will improve the start-up response.

Step 10 – Select the External Biased Resistor for BYPASS Pin

To reduce the no-load input power of the power supply, resistor R5 in Figure 27 of the application example, connected from the feedback capacitor C3 to the BYPASS pin, is recommended. This is applicable to the power supply whose output voltage is higher than $V_{BP(SHUNT)}$.

To achieve lowest no-load power consumption, the current fed into the BYPASS pin should be slightly higher than 120 µA for LNK3202-7 and 150 µA for LNK3208/9. For the best full load efficiency and thermal performance, the current fed into the BYPASS pin should be slightly higher than the current value stated below:

Part Number	Bypass Current
LNK3202	195 µA
LNK3204	222 µA
LNK3205	269 µA
LNK3206	290 µA
LNK3207	340 µA
LNK3208	470 µA
LNK3209	530 µA

Table 11. Bypass Pin Injection Current when MOSFET is Switching.

The BYPASS pin current should not exceed 16 mA ($I_{BP(MAX)}$) at the maximum output voltage (normally when the output voltage is at no-load condition).

Step 11 – Select Pre-Load Resistor

In high-side, direct feedback designs where the minimum load is <3 mA, a pre-load resistor is required to maintain output regulation. This ensures sufficient inductor energy to pull the inductor side of the feedback capacitor C_{FB} to input return via D_{FB}. The value of R_{PL} should be selected to give a minimum output load of 3 mA.

In designs with an optocoupler a Zener diode or reference bias current provides a 1 mA to 2 mA minimum load, preventing "pulse bunching" and increased output ripple at zero load.

Tips for Designs

Start-Up Into Non-Resistive Loads

If the total system capacitance is >100 µF or the output voltage is >12 V, then during start-up the output may fail to reach regulation within 50 ms which can trigger auto-restart protection feature. This may also be true when the load is not resistive, for example, the output is supplying a motor or fan. To increase the start-up time, a soft-start capacitor can be added across the feedback resistor, as shown in Figure 9. The value of this soft-start capacitor is typically in the range of 0.47 µF to 47 µF with a voltage rating of 1.25 × V_O. Addition of this capacitor can lead to instability in some designs that resembles bunching of switching cycles hence this recommendation should be carefully verified by measuring output ripple under different operating conditions.

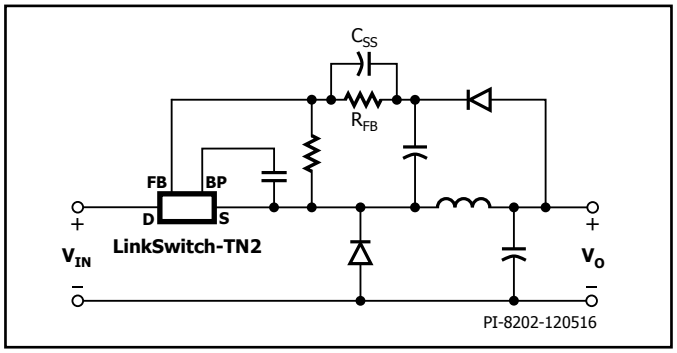


Figure 9. Example Schematic Showing Placement of Soft-Start Capacitor.

Generating Negative and Positive Outputs

In appliance applications there is often a requirement to generate both an AC line referenced positive and negative output. This can be accomplished using the circuit in Figure 10. The two Zener diodes have a voltage rating close to the required output voltage for each rail and ensure that regulation is maintained when one rail is lightly and the other heavily loaded. The LinkSwitch-TN2 circuit is designed as if it were a single output voltage with an output current equal to the sum of both outputs. The magnitude sum of the output voltages in this example is 12 V.

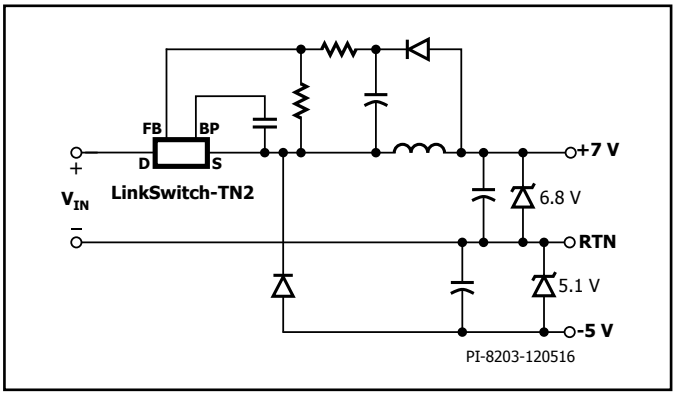


Figure 10. Example Circuit – Generating Dual Output Voltages.

Constant Current Circuit Configuration (LED Driver)

The circuit shown in Figure 11 is ideal for driving constant current loads such as LEDs. It uses the tight tolerance and temperature stable FEEDBACK pin of LinkSwitch-TN2 IC as the reference to provide an accurate output current. To generate a constant current output, the average output current is converted to a voltage by resistor R_{SENSE} and capacitor C_{SENSE} and fed into the FEEDBACK pin via R_{FB} and R_{BIAS}. With the values of R_{BIAS} and R_{FB} as shown, the value of R_{SENSE} should be chosen to generate a voltage drop of 2 V at the required output current. Capacitor C_{SENSE} filters the voltage across R_{SENSE}, which is modulated by inductor ripple current. The value of C_{SENSE} should be large enough to minimize the ripple voltage, especially in M_{DCM} designs. A value of C_{SENSE} is selected such that the time constant (t) of R_{SENSE} and C_{SENSE} is greater than 20 times that of the switching period (15 µs). The peak voltage seen by C_{SENSE} is equal to R_{SENSE} × $I_{LIMIT(MAX)}$. The output capacitor is optional; however with no output capacitor the load will see the full peak current (I_{LIMIT}) of the selected LinkSwitch-TN2 device. Increase the value of C_O (typically in the range of 100 nF to 10 µF) to reduce the peak current to an acceptable level for the load.

If the load is disconnected, feedback is lost and the large output voltage which results may cause circuit failure. To prevent this, a second voltage control loop, D_{FB} and V_{RFB}, can be added as shown in Figure 11. This also requires that capacitor C_O is used in the circuit. The voltage of the Zener is selected as the next standard value above the maximum voltage across the LED string when it is in constant current operation. The same design equations / design spreadsheet can be used as for a standard buck-boost design, with the following additional considerations.

1. V_O = LED V_F × Number of LEDs per string.
2. I_O = LED I_F × Number of strings.
3. Lower efficiency estimate due to R_{SENSE} losses (enter R_{SENSE} into design spreadsheet as inductor resistance).
4. Set R_{BIAS} = 2 kΩ and R_{FB} = 300 Ω.
5. R_{SENSE} = 2/I_O.
6. C_{SENSE} = 20 × (15 µs/R_{SENSE}).
7. Select C_O based on acceptable output ripple current through the load.
8. If the load can be disconnected or for additional fault protection, add voltage feedback components D_{FB} and V_{RFB}, in addition to C_O.

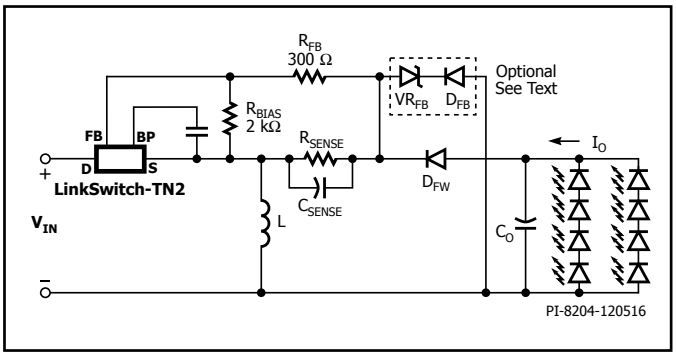


Figure 11. High-Side Buck-Boost Constant Current Output Configuration.

Thermal Environment

To ensure good thermal performance, the SOURCE pin temperature should be maintained below 100 °C, by providing adequate heat sinking. For applications with high ambient temperature (>50 °C), it is recommended to build and test the power supply at the maximum operating ambient temperature and ensure that there is adequate thermal margin. The maximum output current specified in the data sheet is based on specific operating conditions and may need to be thermally derated. Also, it is recommended to use ultrafast (≤35 ns) low reverse recovery diodes at higher operating temperatures (>70 °C). If the device temperature exceeds 85 °C with ambient temperature of 25 °C, it is recommended the next bigger device in the family should be selected for the application.

A battery powered thermocouple meter is recommended to make measurements when the SOURCE pins are a switching node. Alternatively, the ambient temperature may be raised to indicate margin to thermal shutdown.

Recommended Layout Considerations

In the buck or buck-boost converter configuration, since the SOURCE pins in LinkSwitch-TN2 devices are switching nodes, the copper area connected to SOURCE should be minimized to minimize EMI within the thermal constraints of the design.

In the boost configuration, since the SOURCE pins are tied to DC return, the copper area connected to SOURCE can be maximized to improve heat sinking.

Figure 12 are printed circuit board layout design examples for the circuit schematic shown in Figure 27. The loop formed between the LinkSwitch-TN2, inductor (L1), freewheeling diode (D1), and output capacitor (C2) should be kept as small as possible. The loop between the input capacitor C5, IC DRAIN pin, SOURCE pin, freewheeling diode cathode and anode should be as small as possible. The BYPASS pin capacitor C1 (Figure 27) should be located physically close to the SOURCE and BYPASS pins.

Most off-the-shelf inductors are drum core inductors or dog bone inductors. These inductors do not have a good closed magnetic path, and are a source of significant magnetic coupling. They are a source of differential mode noise. To minimize direct coupling from switching nodes, the LinkSwitch-TN2 IC should be placed away from AC input lines. It may be advantageous to place capacitors C4 and C5 in-between LinkSwitch-TN2 device and the AC input. In a drum core inductor, the winding is typically wound in multiple layers. In a given design, result of EMI performance and regulation can change depending on which end of the inductor is connected to the output capacitor and which end is connected to the SOURCE pin of the IC. It is therefore recommended that effect of change of orientation of the inductor be verified and the favorable inductor orientation be used. Once the favorable orientation is determined, the same should be consistently followed on all boards manufactured so as to ensure repeatable performance. Typically inductors are marked to indicate the start and end of the windings. These markings can be used to correctly orient the inductors during assembly.

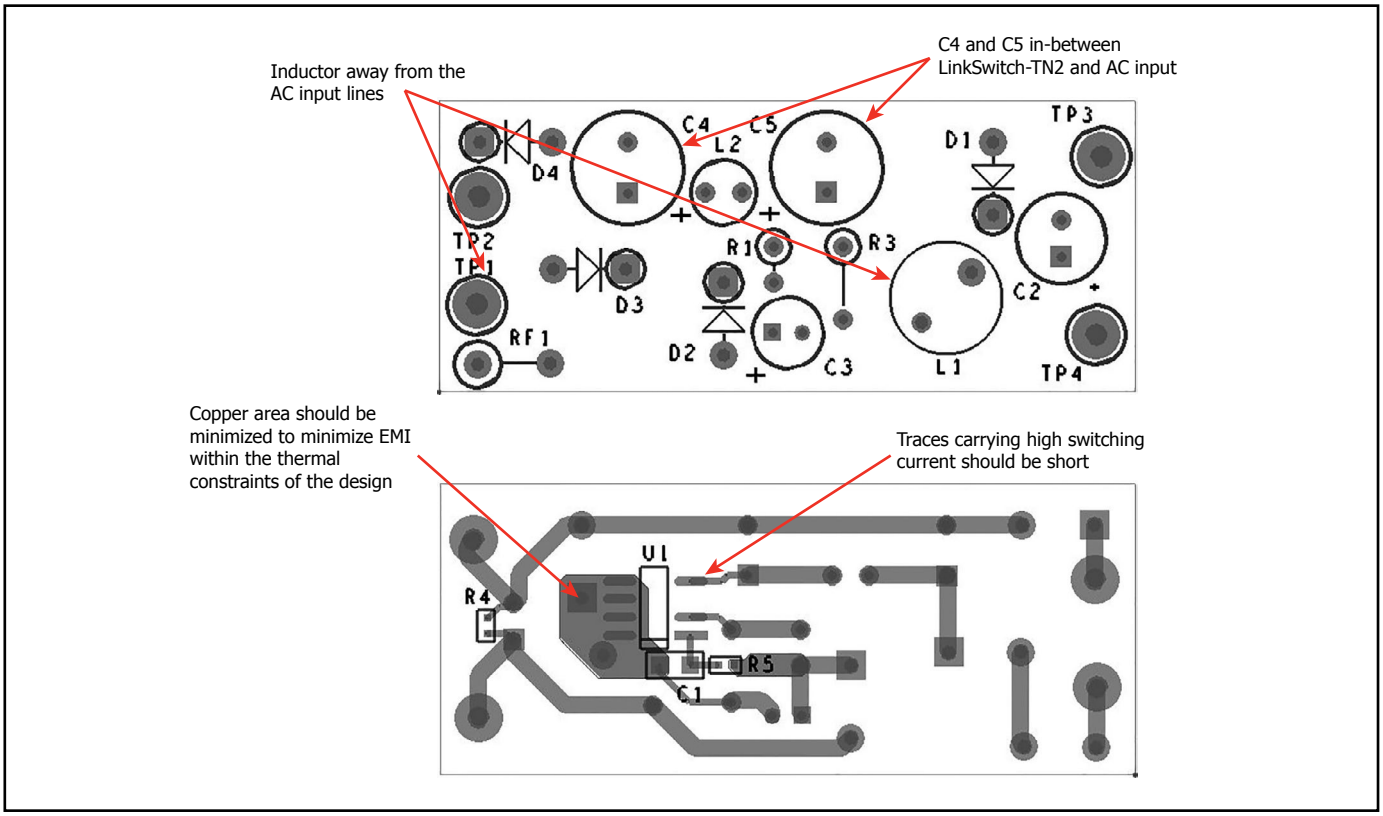
The second rectifier diode D4 is optional, but may be included for better EMI performance and higher line surge withstand capability.

Traces carrying high currents should be as short in length and thick in width as possible. These are the traces which connect the input capacitor, LinkSwitch-TN2 IC, inductor, freewheeling diode, and the output capacitor.

Design for Safety Compliance

Power supplies are required to have capability of withstanding surge voltages which typically are a result of events such as lightning strikes. It is expected that such events do not lead to failure of any components or loss of functionality. Standards such as IEC61000-4-5 defines surge voltage and current waveforms as well as source impedance, which emulate typical worst case transients for testing of protection mechanisms for line connected power circuits and data line connected equipment.

Components of the fusible resistor, EMI filter and the capacitors used in the power supply input stage, help in limiting the voltage and current stress that the components of the power supply are subjected to during these events.



PI-8209-120616

Figure 12. Recommended Printed Circuit Layout for LinkSwitch-TN2 using D Package.

MOVs will often be required to be added at the input of the power supply if the surge level is high (DM surge > 1 kV). These MOVs are placed after the input fuse and help in clamping the voltage at the input of the power supply when a surge event occurs.

The following checklist can be used to ensure that the design is compliant to the applicable requirements:

- Define the target market for LinkSwitch-TN2 converter.
- Determine the equipment class to determine common-mode (CM) and differential-mode (DM) surge levels.
- If DM surge >1000 V, then you will likely need to include an MOV across the AC line at the front-end of the EMI filter
- Select a MOV for North America 115 VAC or universal input with adequate stand-off voltage during normal operation as well as adequate rated surge current and energy capacity.
- An example of selecting an MOV: Assume that you have a North America application within a Class 3 equipment installation for which you need to select a MOV for differential mode protection, connected across the AC line. The DM Spike Energy will be less than 6.9 J. A device rated for 150 VAC continuous operation would provide adequate stand-off voltage for 115 VAC nominal applications. Littlefuse part number V150LA5 provides 25 J and 2500 A surge capability with adequate margin to minimize degraded performance due to accumulated strikes over the life of the MOV. For a universal input design, the V320LA10 provides 48 J and 2500 A surge capability.
- Conduct both common-mode and differential-mode surge tests on the converter and observe voltages across key components and currents where necessary to validate SOA operation of components.
- Verify all voltage and current extremes are within the rated specification of each X and Y capacitor. If not, specify a component with a higher rating.
- Verify surge transient current rating of the diode bridge used.
- Verify MOSFET switch BV rating is greater than surge voltage on switching node. If not, you may need to increase bulk capacitor size to prevent the surge energy from increasing the capacitor voltage to objectionable levels.
- Ensure that bulk capacitor surge voltage rating is not exceeded during testing. If surge voltage rating is exceeded, you may need to increase capacitance. Some capacitors may tolerate higher than the rated surge voltage for short durations however capacitor manufacturers should be consulted for guidance.
- Select an AC line fusible resistor which has an I^2t rating that will accommodate power-on inrush current at maximum line voltage and which is rated for continuous AC line current and will not interrupt due to surge I^2t. Do not oversize the fuse more than necessary to withstand transient currents so as to ensure that the fuse will interrupt line current in the event of a line-to-line MOV failure.

When making measurements on a power supply during a line surge or safety test, care should be taken to ensure that the test equipment is galvanically isolated. If alternate paths for the surge energy are created as a result of connection of test probes, the test result will be incorrect. Care must be taken to use voltage probes that are rated for measurement of high-voltages in excess of the voltages likely to be encountered during the test.

5 V Output With R_{BIAS}

Designer can think that adding R_{BIAS} will not help for a 5 V output LinkSwitch-TN2 buck due to BYPASS Pin (BP) voltage is approximately 5 V. As the load is decrease from full load to minimum load, the output voltage is in increasing trend (full load at 4.88 V and minimum load at 5.13 V). Since at light load the V_O is higher than 5 V, the R_{BIAS} can still help to increase efficiency at light load (Figure 13). At no-load, the R_{BIAS} will help to decease drastically the input power (Figure 14).

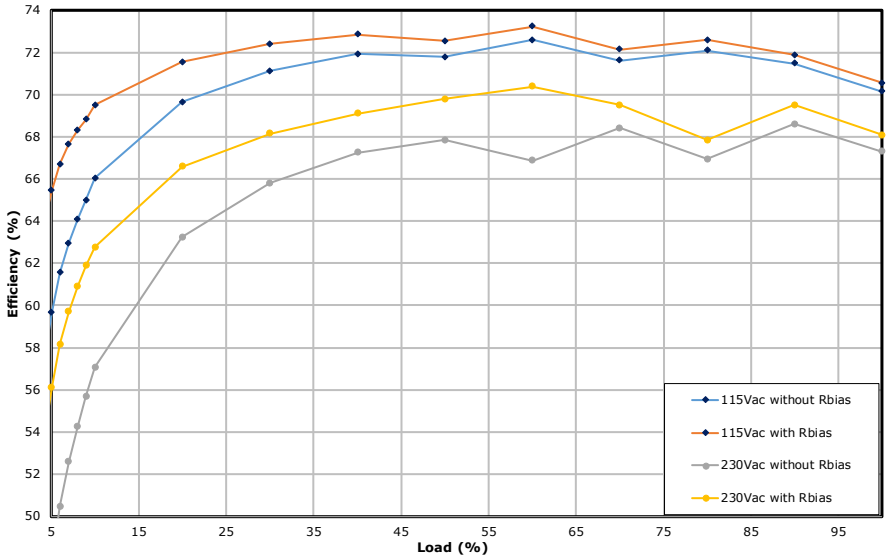


Figure 13. 115 VAC / 230 VAC Load Efficiency with and without R_{BIAS}.

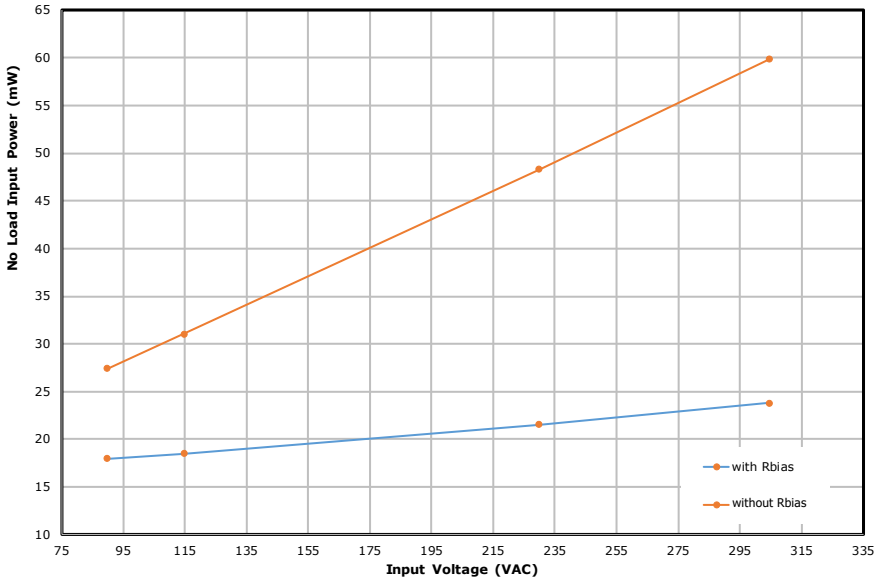


Figure 14. No-Load Input Power with and without R_{BIAS}.

LNK3207/8/9 EMI and Thermals Mitigation

LNK3207/8/9 have a much higher output power capability. LinkSwitch-TN2's SOURCE trace acts as a heat sink to the device. The higher the power capability the larger the SOURCE trace in order to lower down the device thermals. Larger SOURCE trace will worsen EMI.

- Larger SOURCE Trace AREA = Bad EMI and Low device thermals
- Smaller SOURCE Trace Area = Good EMI and High device thermals

Solution to this concern is to use a double sided PCB. By reducing the bottom SOURCE trace area by half and transferring to the top side will make the effective radiating area to be half (Figure 15). This will improve EMI response. PCB vias will be used to interconnect top and bottom SOURCE trace. For efficient thermal transfer between top and bottom, PCB vias should be solder filled. Due to the added vias, IC thermal will be slightly high as compare to single sided but still in manageable numbers (Figures 16-19, Table 12).

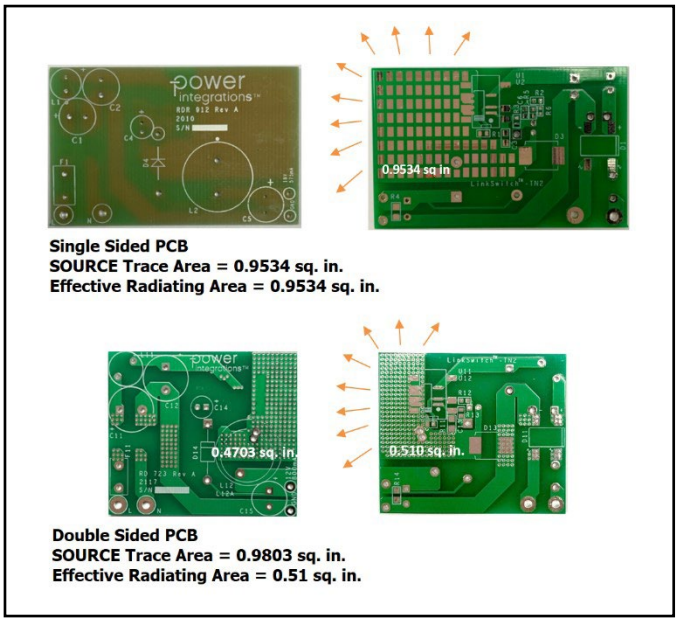


Figure 15. Single Side PCB and Double Sided PCB with the same SOURCE Trace Area.

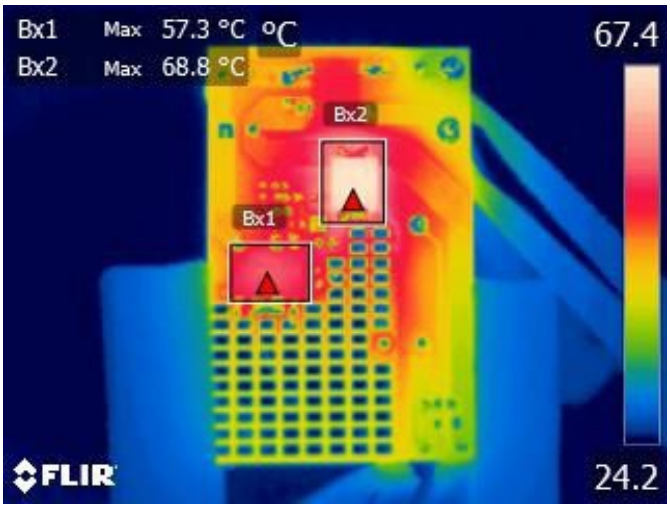


Figure 16. 85 VAC, I_o = 800 mA (Full Load) LNK3209G: 57.3 °C.

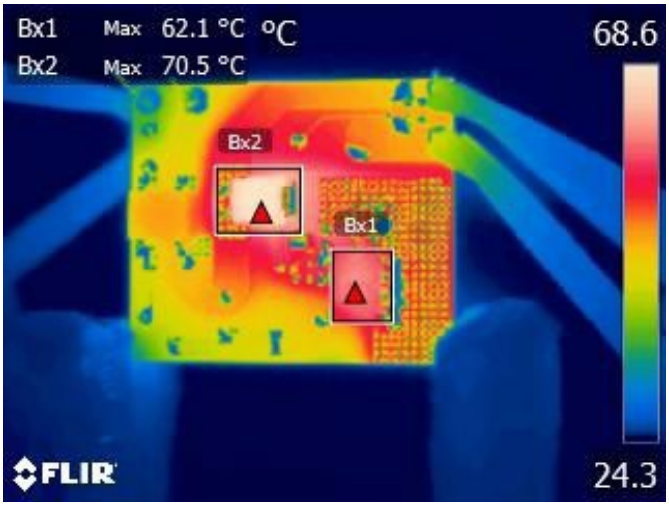


Figure 17. 85 VAC, I_o = 800 mA (Full Load) LNK3209G: 62.1 °C.

Figure 18. 265 VAC, I_O = 800 mA (Full Load) LNK3209G: 58.7 °C

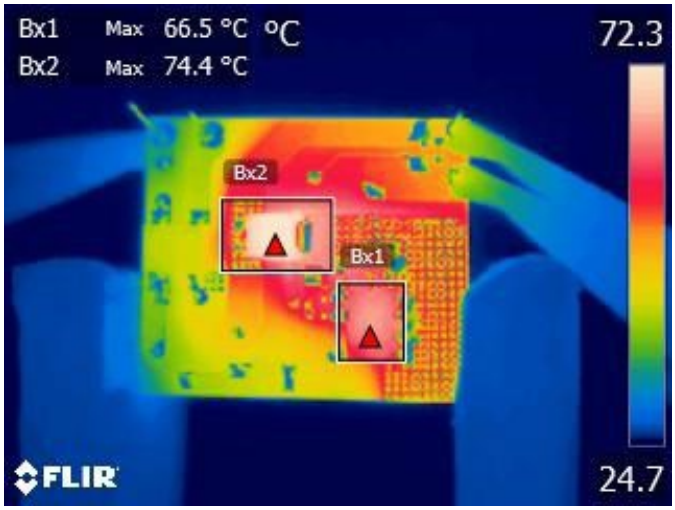


Figure 19. 265 VAC, I_O = 800 mA (Full Load) LNK3209G: 66.5 °C

Input Voltage	PCB	SOURCE Trace Area	Measured Temperature		Normalize to 25 °C	
			Ambient	LNK3209G	Ambient	LNK3209G
85 VAC	Single Sided	Bottom = 0.9534 in²	24.2 °C	57.3 °C	25 °C	58.1 °C
	Double Sided	Top = 0.47 in²; Bottom = 0.51 in²	24.3 °C	62.1 °C	25 °C	62.8 °C
265 VAC	Single Sided	Bottom = 0.9534 in²	24.2 °C	58.7 °C	25 °C	59.5 °C
	Double Sided	Top = 0.47 in²; Bottom = 0.51 in²	24.7 °C	66.5 °C	25 °C	66.8 °C

Table 12. Thermal Difference Between Single Sided and Double Sided PCB with Comparable SOURCE Trace Area.

Worst conducted EMI response can be seen on a bigger SOURCE trace area PCB as shown in Table 13. Conducted EMI is much lower using double sided PCB with the lowest top and bottom SOURCE trace area. As the SOURCE trace area is increased, the effective radiating area increases that resulted to worsening of conducted EMI response.

PCB	SOURCE Trace Area		Conducted EMI Margin (Float)			
	Top	Bottom	115 VAC L	115 VAC N	230 VAC L	230 VAC N
Double Sided Version 1 1.68″ x 1.46″	0.4703	0.5102	13.13 dB	12.26 dB	7.59 dB	6.51 dB
Double Sided Version 2 1.83″ x 1.46″	0.7051	0.768	11.91 dB	11.75 dB	6.54 dB	6.42 dB
Double Sided Version 3 2.09″ x 1.46″	0.9748	1.0374	10.76 dB	10.57 dB	4.42 dB	4.14 dB
Double Sided Version 4 2.33″ x 1.46″	1.2273	1.2901	10.03 dB	9.32 dB	2.73 dB	1.80 dB

Table 13. EMI Difference Between Single Sided and Double Sided PCB with Comparable SOURCE Trace Area.

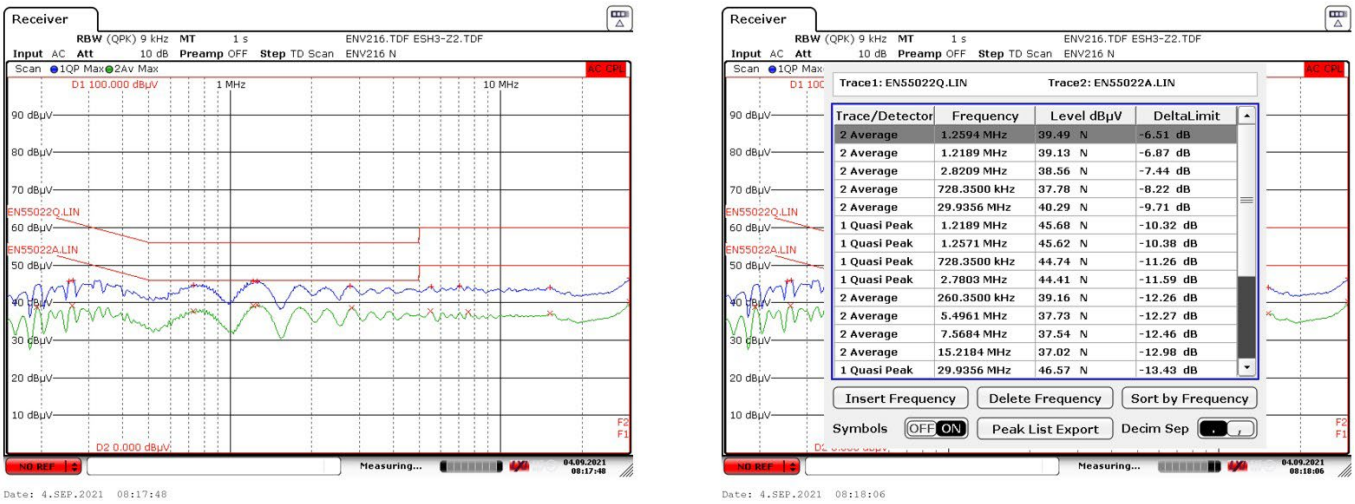


Figure 20. PCB Version 1: 230 VAC, I_O = 800 mA (Full Load), Floating Neutral.

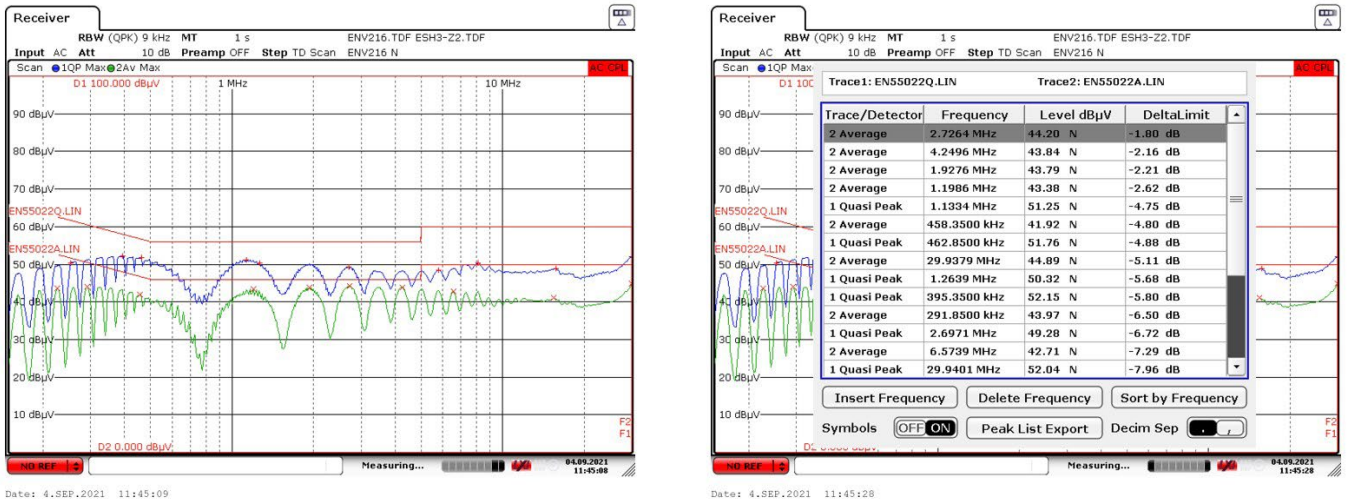


Figure 21. PCB Version 4: 230 VAC, I_O = 800 mA (Full Load), Floating Neutral.

Special Consideration for LNK3207/8/9

LNK3207/8/9 are the only devices in the LinkSwitch-TN2 product family that have current limit state machine (see Figures 2 to 5). As the output load is changed, the current limit also transitions to a different state. In some cases, pulse grouping may occur if the current limit is stuck from going back and forth one state change to another. This condition is more prone to happen at high-line input, and with heavier or more CCM load.

Figure 22 shows the recommended circuit when using LNK3207/8/9 in high-side buck or buck-boost applications. Resistor R5 is added and connected in series with feedback capacitor C4.

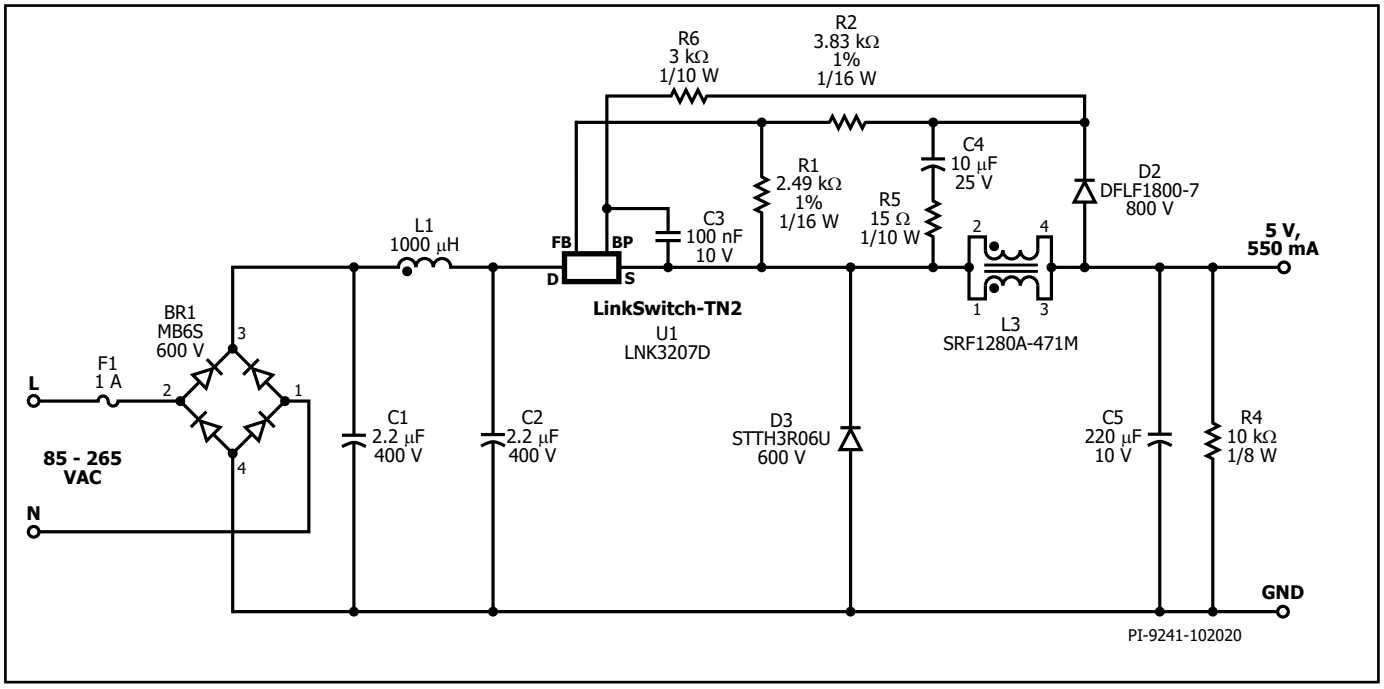


Figure 22. Schematic 85 VAC - 265 VAC 6 V / 1 A.

With R5 shorted, the waveforms looked normal at 250 mA load current (Figure 23). At 400 mA load (Figure 24), huge oscillation can be seen on the output voltage due to pulse grouping of the Drain current. This condition not only causes huge output voltage ripple but it can also result to higher audible noise.

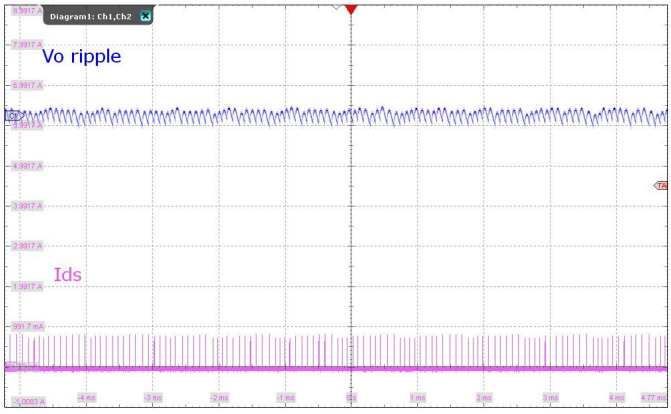


Figure 23. 265 VAC 50 Hz 5 V / 250 mA, R5 Shorted.

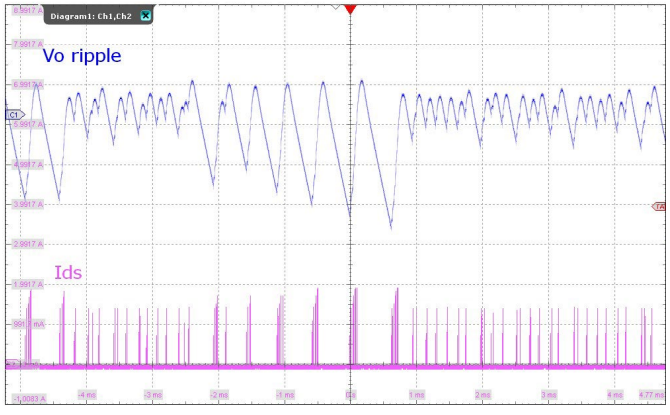


Figure 24. 265 VAC 50 Hz 5 V / 400 mA, R5 Shorted.

With R5 connected, Figure 25 and 26 show that the oscillation is gone.

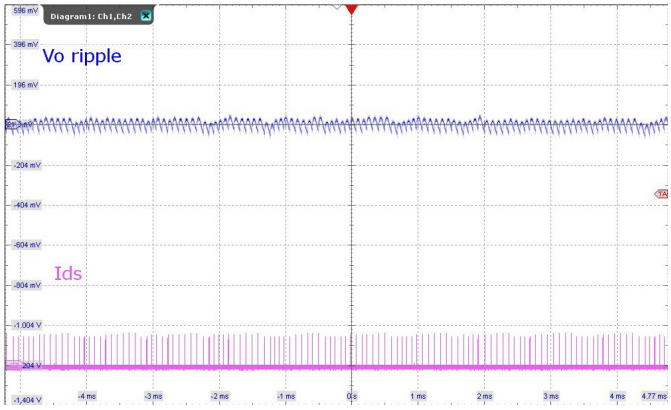


Figure 25. 265 VAC 50 Hz 5 V / 250 mA, R5 = 15 Ω.

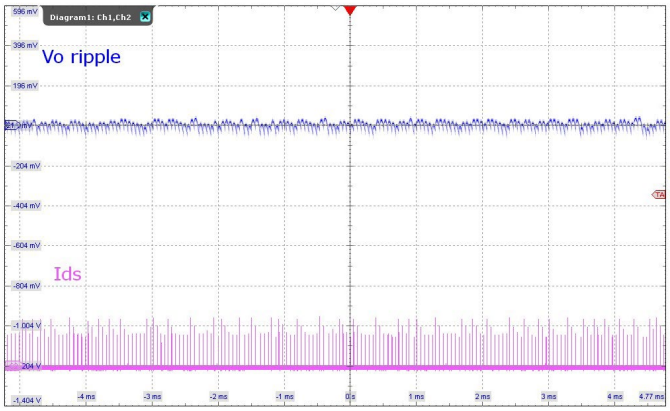


Figure 26. 265 VAC 50 Hz 5 V / 400 mA, R5 = 15 Ω.

The drawback with this circuit is the slightly worse load regulation. Thus, choose a value between 4.7 Ω and 30 Ω to balance between regulation and output ripple.

Appendix A – Application Example

A 1.44 W Universal Input Buck Converter

The circuit shown in Figure 27 is a typical implementation of a 12 V, 120 mA non-isolated power supply used in appliance control such as rice cookers, dishwashers or other white goods. This circuit may also be applicable to other applications such as night-lights, LED drivers, electricity meters, and residential heating controllers, where a non-isolated supply is suitable.

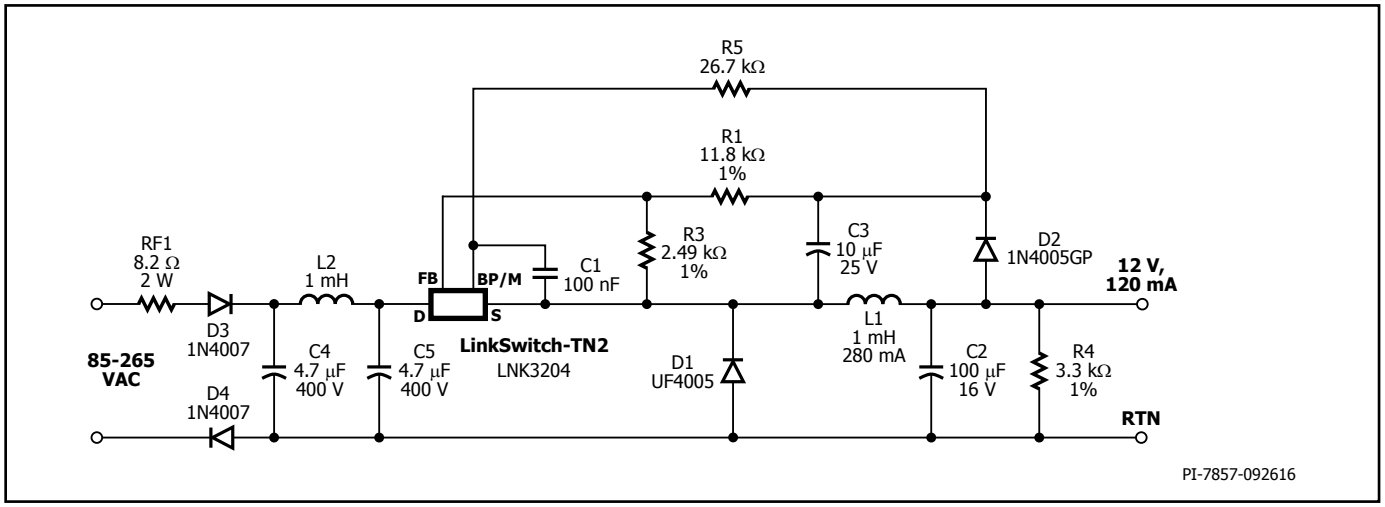


Figure 27. Universal Input, 12 V, 120 mA Constant Voltage Power Supply using LinkSwitch-TN2.

Appendix B

Calculations for Inductor Value for Buck and Buck-Boost Topologies

There is a minimum value of inductance that is required to deliver the specified output power, regardless of line voltage and operating mode.

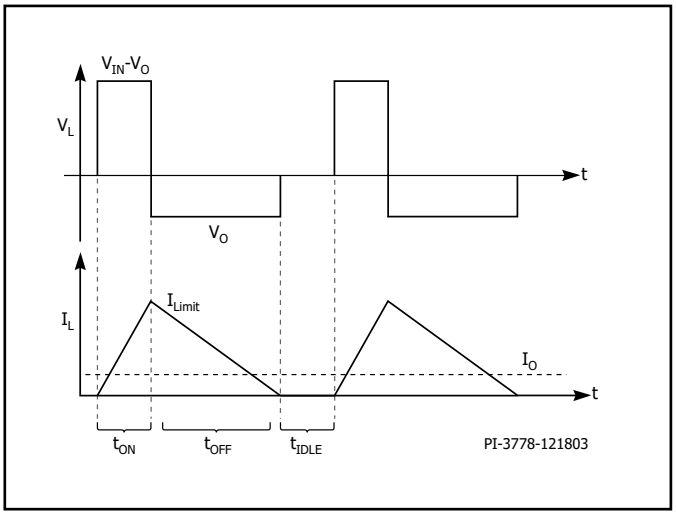


Figure 28. Inductor Voltage and Inductor Current of a Buck Converter in DCM.

As a general case, Figure 28 shows the inductor current in discontinuous conduction mode (DCM). The following expressions are valid for both CCM as well as DCM operation. There are three unique intervals in DCM as can be seen from Figure 28. Interval t_{ON} is when the LinkSwitch-TN2 IC is ON and the freewheeling diode is OFF. Current ramps up in the inductor from an initial value of zero. The peak current is the current limit I_{LIMIT} of the device. Interval t_{OFF} is when the LinkSwitch-TN2 IC is OFF and the freewheeling diode is ON. Current ramps down to zero during this interval. Interval t_{IDLE} is when both the LinkSwitch-TN2 IC and freewheeling diode are OFF, and the inductor current is zero.

In CCM, this idle state does not exist and thus $t_{IDLE} = 0$.

We can express the current swing at the end of interval t_{ON} in a buck converter as:

$$\Delta I(t_{ON}) = I_{RIPPLE} = \frac{V_{MIN} - V_{DS} - V_O}{L_{MIN}} \times t_{ON} \quad \text{(C1)}$$

$$I_{RIPPLE} = 2 \times (I_{LIMIT\_MIN} - I_O) \quad t_{IDLE} = 0 (for\ CCM) \quad \text{(C2)}$$

$$I_{RIPPLE} = (I_{LIMIT\_MIN,}) \quad t_{IDLE} > 0 (for\ MDCM) \quad \text{(C3)}$$

where
I_{RIPPLE} = Inductor ripple current
I_{LIMIT_MIN} = Minimum current limit
V_{MIN} = Minimum DC bus voltage
V_{DS} = On-state Drain to Source voltage drop
V_O = Output voltage
L_{MIN} = Minimum inductance

Similarly, we can express the current swing at the end of interval t_{OFF} as:

$$\Delta I(t_{OFF}) = I_{RIPPLE} = \frac{V_O + V_{FD}}{L_{MIN}} \times t_{OFF} \quad \text{(C4)}$$

The initial current through the inductor at the beginning of each switching cycle can be expressed as:

$$I_{INITIAL} = I_{LIMIT\_MIN} - I_{RIPPLE} \quad \text{(C5)}$$

The average current through the inductor over one switching cycle is equal to the output current I_O. This current can be expressed as:

$$I_O = \frac{1}{T_{SW\_MAX}} \left(\frac{1}{2} \times (I_{LIMIT\_MIN} + I_{INITIAL}) \times t_{ON} + \frac{1}{2} \times (I_{LIMIT\_MIN} + I_{INITIAL}) \times t_{OFF} + 0 \times t_{IDLE} \right) \quad \text{(C6)}$$

Where

I_O = Output current.
T_{SW_MAX} = The switching interval corresponding to minimum switching frequency F_{SMIN}.

Substituting for t_{ON} and t_{OFF} from equations (C1) and (C4) we have:

$$I_O = \frac{1}{T_{SW\_MAX}} \left(\frac{1}{2} \times (I_{LIMIT\_MIN} + I_{INITIAL}) \times \frac{I_{RIPPLE} \times L_{MIN}}{V_{MIN} - V_{DS} - V_O} + \frac{1}{2} \times (I_{LIMIT\_MIN} + I_{INITIAL}) \times \frac{I_{RIPPLE} \times L_{MIN}}{V_O + V_{FD}} + t_{IDLE} \right) \quad \text{(C7)}$$

$$L_{MIN} = \frac{2 \times (V_O + V_{FD}) \times I_O \times (V_{MIN} - V_{DS} - V_O)}{(I_{LIM\_MIN}^2 - I_{INITIAL}^2) \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD})} \quad \text{(C8)}$$

For MDCM design, $I_{INITIAL} = 0$, $I_{RIPPLE} = I_{LIMIT\_MIN}$.

$$L_{MIN} = \frac{2 \times (V_O + V_{FD}) \times I_O \times (V_{MIN} - V_{DS} - V_O)}{I_{LIM\_MIN}^2 \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD})} \quad \text{(C9)}$$

For CCM design, $t_{IDLE} = 0$.

$$I_O = \frac{1}{2} \times (I_{LIMIT\_MIN} + I_{INITIAL}) \quad \text{(C10)}$$

$$I_{INITIAL} = I_{LIM\_MIN} \quad \text{(C11)}$$

$$L_{MIM} = \frac{(V_O + V_{FD}) \times (V_{MIN} - V_{DS} - V_O)}{2 \times (I_{LIM\_MIN} - I_O) \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD})} \quad \text{(C12)}$$

For output voltages greater than 20 V, use V_{MAX} for calculation of L_{MIN} (Equation C8). For output voltages less than 20 V, use V_{MIN} for calculation of L_{MIN} to compensate for current limit delay time overshoot.

This however does not account for the losses within the inductor (resistance of winding and core losses) and the freewheeling diode, which will limit the maximum power delivering capability and thus reduce the maximum output current. The minimum inductance must compensate for these losses in order to deliver specified full load power. An estimate of these losses can be made by estimating the total losses in the power supply, and then allocating part of these losses to the inductor and diode. This is done by the loss factor K_{LOSS} which increases the size of the inductor accordingly. Furthermore, typical inductors for this type of application are bobbin core or dog bone chokes. The specified current rating refer to a temperature rise of 20 °C or 40 °C and to an inductance drop of 10%. We must

incorporate an inductance tolerance factor K_{L_TOL} within the expression for minimum inductance, to account for this manufacturing tolerance. The typical inductance value thus can be expressed as:

$$L_{TYP} = \frac{(1+K_{L\_TOL}) \times L_{MIN}}{K_{LOSS}} \quad \text{(C13)}$$

where

K_{LOSS} is a loss factor, which accounts for the off-state total losses of the inductor.

K_{L_TOL} is the inductor tolerance factor and can be between 10% and 20%. A typical value is 0.15. With this typical inductance we can express maximum output power as:

$$P_{O\_MAX} = L_{TYP} \times FS_{MIN} \times (I_{LIMIT\_MIN}^2 - I_{INITIAL}^2) \times \frac{V_O \times (V_{MIN} - V_{DS} + V_{FD})}{2 \times (V_{MIN} - V_{DS} - V_O) \times (V_O + V_{FD})} \times \frac{K_{LOSS}}{(1 + K_{L\_TOL})} \quad \text{(C14)}$$

Similarly for buck-boost topology the expressions for L_{TYP} and P_{O_MAX} are:

$$L_{TYP} = 2(1 + K_{L\_TOL}) \times (V_O + V_{FD}) \times \frac{I_O \times (V_{MIN} - V_{DS})}{K_{LOSS} \times (I_{LIMIT\_MIN}^2 - I_{INITIAL}^2) \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD} + V_O)} \quad \text{(C15)}$$

$$P_{O\_MAX} = L_{TYP} \times FS_{MIN} \times (I_{LIMIT\_MIN}^2 - I_{INITIAL}^2) \times \frac{V_O \times (V_{MIN} - V_{DS} + V_{FD} + V_O)}{2 \times (V_{MIN} - V_{DS}) \times (V_O + V_{FD})} \times \frac{K_{LOSS}}{(1 + K_{L\_TOL})} \quad \text{(C16)}$$

Average Switching Frequency

Since LinkSwitch-TN2 uses an on-off type of control, the frequency of switching is non-uniform due to cycle skipping. We can average this switching frequency by substituting the maximum power as the output power in Equation C14. Simplifying, we have:

$$FS_{AVG} = 2 \times (1 + K_{L\_TOL}) \times (V_O + V_{FD}) \times \frac{I_O \times (V_{MIN} - V_{DS} - V_O)}{K_{LOSS} \times (I_{LIMIT\_MIN}^2 - I_{INITIAL}^2) \times L_{TYP} \times (V_{MIN} - V_{DS} + V_{FD})} \quad \text{(C17)}$$

Similarly for buck-boost converter, simplifying Equation C16 we have:

$$FS_{AVG} = 2(1 + K_{L\_TOL}) \times (V_O + V_{FD}) \times \frac{I_O \times (V_{MIN} - V_{DS})}{K_{LOSS} \times (I_{LIMIT\_MIN}^2 - I_{INITIAL}^2) \times L_{TYP} \times (V_{MIN} - V_{DS} + V_{FD} + V_O)} \quad \text{(C18)}$$

Calculation of RMS Currents

The RMS current value through the inductor is mainly required to ensure that the inductor is appropriately sized and will not overheat. Also, RMS currents through the LinkSwitch-TN2 IC and freewheeling diode are required to estimate losses in the power supply. Assuming CCM operation, the initial current in the inductor in steady state is given by:

$$I_{INITIAL} = I_{LIM\_MIN} - \frac{V_O + V_{FD}}{L_{TYP}} \times t_{OFF} \quad \text{(C19)}$$

t_{OFF} is when MOSFET is off.

For DCM operation this initial current will be zero.

The current through the LinkSwitch-TN2 as a function of time is given by:

$$i_{SW}(t) = I_{INITIAL} + \frac{V_{MIN} - V_{DS} - V_O}{L_{TYP}} \times t, 0 < t \leq t_{ON} \quad \text{(C20)}$$

$$i_{SW}(t) = 0, t_{ON} < t \leq T \quad \text{(C21)}$$

t_{ON} is when MOSFET is on.

The current through the freewheeling diode as a function of time is given by:

$$i_D(t) = 0, 0 < t \leq t_{ON} \quad \text{(C22)}$$

$$i_D(t) = I_{ILIM\_MIN} - \frac{V_O + V_{FD}}{L_{TYP}} \times t, t_{ON} < t \leq t_{OFF} \quad \text{(C23)}$$

$$i_D(t) = 0, t_{OFF} < t \leq T \quad \text{(C24)}$$

t_{OFF} is when freewheeling diode is on.

And the current through the inductor as a function of time is given by:

$$i_L(t) = i_{SW}(t) + i_D(t) \quad \text{(C25)}$$

From the definition of RMS currents we can express the RMS currents through the switch, freewheeling diode and inductor as follows:

$$i_{SW\_RMS} = \sqrt{\frac{1}{T_{AVG}} \int_0^T i_{SW}(t)^2 \times dt} \quad \text{(C26)}$$

$$i_{D\_RMS} = \sqrt{\frac{1}{T_{AVG}} \int_0^T i_D(t)^2 \times dt} \quad \text{(C27)}$$

$$i_{L\_RMS} = \sqrt{\frac{1}{T_{AVG}} \int_0^T (i_{SW}(t) + i_D(t))^2 \times dt} \quad \text{(C28)}$$

Since the switch and freewheeling diode currents fall to zero during the turn-off and turn-on intervals respectively, the RMS inductor current is simplified to:

$$i_{L\_RMS} = \sqrt{i_{SW}^2 + i_D^2} \quad \text{(C29)}$$

Table C1 lists the design equations for important parameters using the buck and buck-boost topologies.

Parameter	Buck	Buck-Boost
L_{TYP}	$L_{TYP} = \frac{2(1+K_{L\_TOL}) \times (V_O + V_{FD}) \times I_O \times (V_{MIN} - V_{DS} - V_O)}{K_{LOSS} \times (I_{LIM\_MIN}^2 - I_{INITIAL}^2) \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD})}$	$L_{TYP} = \frac{2(1+K_{L\_TOL}) \times (V_O + V_{FD}) \times I_O \times (V_{MIN} - V_{DS})}{K_{LOSS} \times (I_{LIM\_MIN}^2 - I_{INITIAL}^2) \times FS_{MIN} \times (V_{MIN} - V_{DS} + V_{FD} + V_O)}$
FS_{AVG}	$FS_{AVG} = \frac{2 \times (1+K_{L\_TOL}) \times (V_O + V_{FD}) \times I_O \times (V_{MIN} - V_{DS} - V_O)}{K_{LOSS} \times (I_{LIM\_MIN}^2 - I_{INITIAL}^2) \times L_{TYP} \times (V_{MIN} - V_{DS} + V_{FD})}$	$FS_{AVG} = \frac{2(1+K_{L\_TOL}) \times (V_O + V_{FD}) \times I_O \times (V_{MIN} - V_{DS})}{K_{LOSS} \times (I_{LIM\_MIN}^2 - I_{INITIAL}^2) \times L_{TYP} \times (V_{MIN} - V_{DS} + V_{FD} + V_O)}$
$i_{SW}(t)$ LinkSwtich-TN2 Current	$i_{SW}(t) = I_{INITIAL} + \frac{V_{MIN} - V_{DS} - V_O}{L_{TYP}} \times t, 0 < t \leq t_{ON}$ $i_{SW}(t) = 0, t_{ON} < t \leq T$	$i_{SW}(t) = I_{INITIAL} + \frac{V_{MIN} - V_{DS}}{L_{TYP}} \times t, 0 < t \leq t_{ON}$ $i_{SW}(t) = 0, t_{ON} < t \leq T$
$i_D(t)$ Diode Forward Current	$i_D(t) = 0, 0 < t \leq t_{ON}$ $i_D(t) = I_{LIMIT\_MIN} - \frac{V_O + V_{FD}}{L_{TYP}} \times t, t_{ON} < t \leq t_{OFF}$ $i_D(t) = 0, t_{OFF} < t \leq T$	$i_D(t) = 0, 0 < t \leq t_{ON}$ $i_D(t) = I_{LIMIT\_MIN} - \frac{V_O + V_{FD}}{L_{TYP}} \times t, t_{ON} < t \leq t_{OFF}$ $i_D(t) = 0, t_{OFF} < t \leq T$
$i_L(t)$ Inductor Current	$i_L(t) = i_{SW}(t) + i_D(t)$	$i_L(t) = i_{SW}(t) + i_D(t)$
Max Drain Voltage	V_{MAX}	$V_{MAX} + V_O$

Table C1. Circuit Characteristics for Buck and Buck-Boost Topologies.

Appendix C – Protection Feature for Flyback Applications

Hysteretic Output Overvoltage Protection

In flyback topology, the output overvoltage protection provided by the LinkSwitch-TN2 IC uses auto-restart that is triggered by a current >$I_{BP(SD)}$ into the BYPASS pin. To prevent inadvertent triggering of this feature, in addition to an internal filter, the BYPASS pin capacitor provides external filtering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and BYPASS pins of the device.

The OVP function can be realized in a non-isolated flyback converter by connecting a Zener diode from the output to the BYPASS pin. The circuit example shown in Figure 29 describes a simple method for implementing the output overvoltage protection. Additional filtering for the OVP detection feature, can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the OVP Zener diode. The resistor in series with the OVP Zener diode also limits the maximum current into the BYPASS pin. The current should be limited to less than 16 mA.

During a fault condition resulting from loss of feedback, the output voltage will rapidly rise above the nominal voltage. A voltage at the output that exceeds the sum of the voltage rating of the Zener diode and the BYPASS pin voltage will cause a current in excess of $I_{BP(SD)}$ injected into the BYPASS pin, which will trigger the auto-restart and protect the power supply from overvoltage.

Line Overvoltage Protection

In a flyback converter configuration, during the power MOSFET on-time, the LinkSwitch-TN2 IC can sense indirectly the DC bus overvoltage condition by monitoring the current flowing into the FEEDBACK pin depending on circuit configuration. Figure 30 shows one possible circuit implementation. During the power MOSFET on-time, the voltage across the secondary winding is proportional to the voltage across the primary winding. The current flowing through emitter and base of transistor Q3 is therefore directly proportional to the V_{BUS} voltage.

$$V_{PRI} = V_{BUS} - V_{DS} \quad \text{(D1)}$$

V_{DS} is much smaller compared to the bus voltage which can be neglected.

The voltage across the secondary winding is proportional to the voltage across the primary winding.

$$V_{SEC} = \frac{V_{PRI}}{n} \quad \text{(D2)}$$

$$-V_{BP} + V_{Q3(EB)} + V_{D3} + V_{VR3} + V_{R3} = V_{SEC} \quad \text{(D3)}$$

The voltage across the Zener diode VR3 is therefore dependent on V_{BUS}. When the line voltage is higher than its threshold and the Zener diode VR3 is turned on, transistor Q3 is turned on and current will flow into FEEDBACK pin from the BYPASS pin capacitor through transistor Q3. When the fed current is higher than FEEDBACK pin

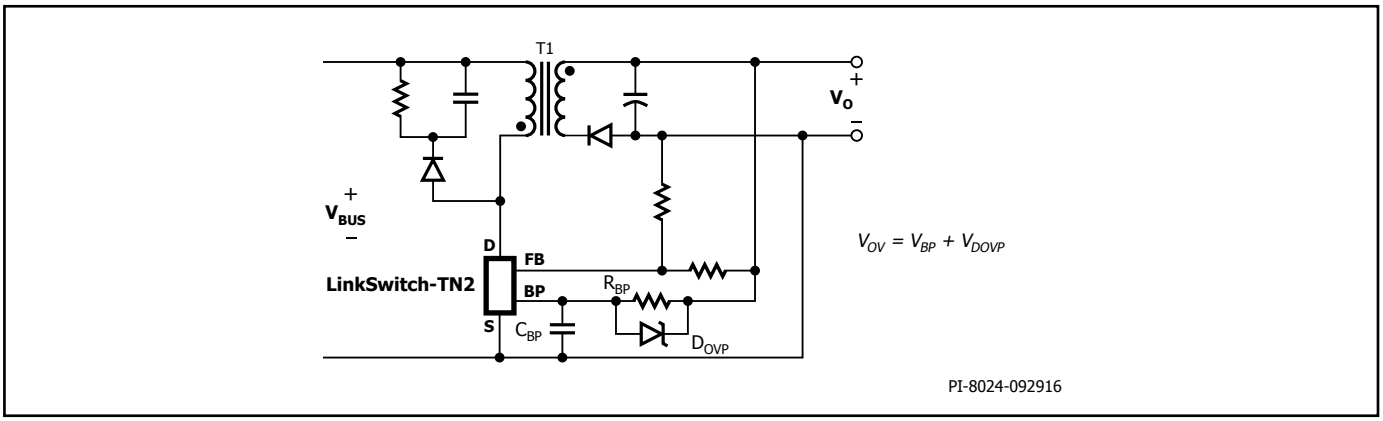


Figure 29. Non-Isolated Flyback Converter with Output Overvoltage Protection.

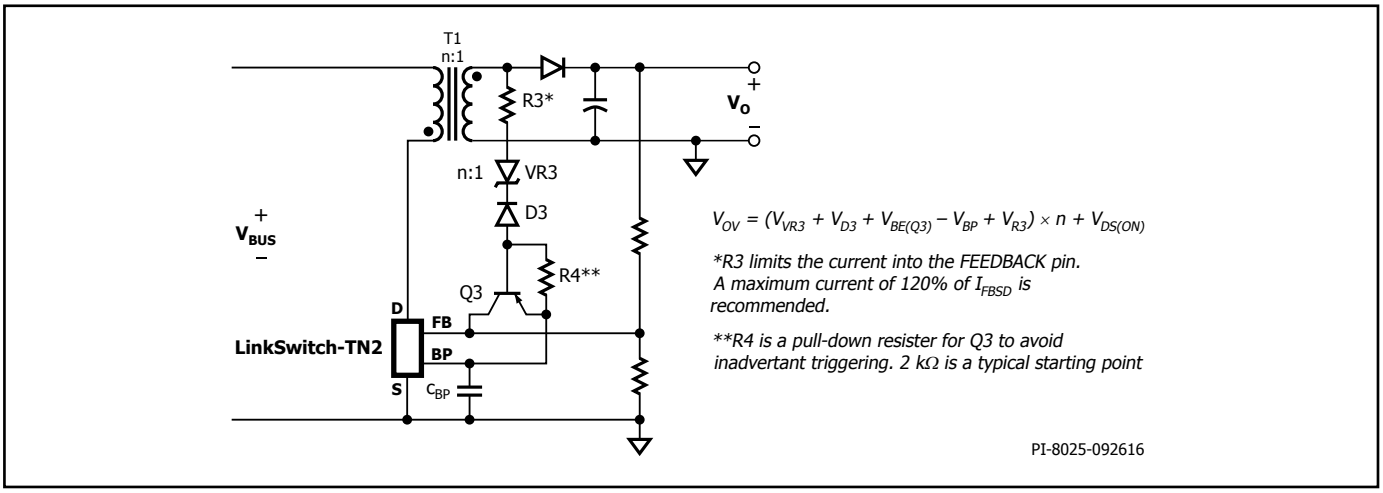


Figure 30. Line-Sensing for Overvoltage Protection by using FEEDBACK Pin.

instant shutdown current $I_{FB(SD)}$ for at least 2 consecutive switching cycles, the line overvoltage protection will be triggered and the LinkSwitch-TN2 IC will go into auto-restart mode.

The threshold for the bus overvoltage is:

$$V_{OV} = (-V_{BP} + V_{Q3(EB)} + V_{D3} + V_{VR3} + V_{R3}) \times n + V_{DS} \quad \text{(D4)}$$

Indirect line sensing minimizes power dissipation otherwise incurred in a typical primary side line overvoltage detection circuit.

Resistor R4 is used as a weak pull-down resistor to help avoid inadvertent conduction of Q3 during normal operation. A 2 kΩ resistor can be used for R4. Based on the selection of the zener diode and transistor, the value of R4 may need to be adjusted. R3 is used to limit the current into the FEEDBACK pin. The current through resistor R3 is equal to the sum of current through R4 and current through emitter and base of Q3, which is:

$$I_{R3} = I_{Q3(EB)} + I_{R4} \quad \text{(D5)}$$

From equation D4:

$$I_{R3} = \frac{V_{R3}}{R3} = \frac{\frac{(V_{BUS} - V_{DS})}{N} + V_{BP} - V_{Q3(EB)} - V_{D3} - V_{VR3}}{R_3} \quad \text{(D6)}$$

And

$$I_{R4} = \frac{V_{BE(Q3)}}{R_4} \quad \text{(D7)}$$

From the equation D6 and D7:

$$I_{Q3(EB)} = \frac{\frac{(V_{BUS} - V_{DS})}{N} + V_{BP} - V_{Q3(BE)} - V_{D3}}{R3} - \frac{V_{BE(Q3)}}{R4} \quad \text{(D7)}$$

The current into FEEDBACK pin is the collector current of Q3 if the transistor is not saturated, which is calculated as:

$$I_{Q3(EC)} = h_{FE} \times I_{Q3(EB)} = h_{FE} \times \left[\frac{\frac{(V_{BUS} - V_{DS})}{N} + V_{BP} - V_{Q3(BE)} - V_{D3} - V_{VR3}}{R3} - \frac{V_{BE(Q3)}}{R4} \right] \quad \text{(D8)}$$

The current of $I_{Q3(EC)}$ should not exceed 120% of $I_{FB(SD)}$ in order to limit the current into the FEEDBACK pin.

In order to have accurate line OV threshold voltage and also for good efficiency, regulation performance and stability, the transformer leakage inductance should be minimized. Low leakage will minimize ringing on the secondary winding and provide accurate line OVP detection. The current into the FEEDBACK pin is sampled and compared to $I_{FB(SD)}$ typically 280 ns after the high-voltage power MOSFET is turned on.

In some designs if the ringing at the secondary winding is longer than 280 ns, a RC snubber across the rectifier diode may be needed to damp the ringing to ensure precise detection of line voltage.

Below is an example with 33 V Zener (VR3) BZX74-C33, and the threshold is at 308 V. When the bus voltage is higher than the threshold, the power supply goes into auto-restart. The first time a fault is asserted the off-time is 150 ms ($t_{AR(OFF)}$ – first off period). If the fault condition persists, subsequent off-times are 1500 ms long ($t_{AR(OFF)}$ subsequent periods).

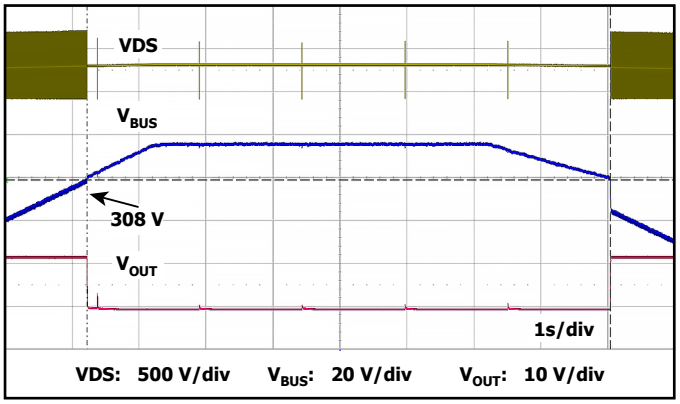


Figure 31. Indirect Line-Sensing for Overvoltage Protection Result.

Appendix D. Low Input Voltage Application

In some application, it is required that the power supply needs to be operate in a very low voltage. Low input voltage power capability for buck converter is shown on Table D.1.

LinkSwitch-TN2	V_{IN_MIN} (V_{DC})	V_O (V)	I_O (mA)	L_O (µH)	P_O (W)
LNK3202	25	5	80	2200	0.40
	25	12	80	2200	0.96
	30	15	80	3300	1.20
LNK3204	25	5	170	1000	0.85
	25	12	165	1000	1.98
	30	15	165	1000	2.48
LNK3205	25	5	270	680	1.35
	25	12	270	820	3.24
	30	15	270	1000	4.05
LNK3206	25	5	360	680	1.80
	25	12	360	680	4.32
	30	15	360	820	5.40
LNK3207	25	5	575	470	2.88
	25	12	400	470	4.80
	30	15	400	470	6.00
LNK3208	25	5	775	330	3.88
	25	12	550	330	6.60
	30	15	600	330	9.00
LNK3209	25	5	1000	330	5.00
	25	12	750	330	9.00
	30	15	750	330	11.25

Table D.1 Buck Converter Power Capability at Low Input Voltage.

At low input voltage, duty cycle will be higher to deliver the required output power. A higher duty cycle will increase conduction loss of the FET. This will lead to increase in IC temperature. It is recommended to build and test the power supply to ensure that there is adequate thermal margin.

For Buck topology, it is not recommend operating the power supply at no-load and low bulk voltage (below 50 V). This will result to a high output voltage that can possibly damage the output capacitor. It is recommended to add a Resistor-Zener circuit in the output to avoid exceeding voltage rating of the output capacitor (Figure 32). The Resistor-Zener circuit will act as active pre-load.

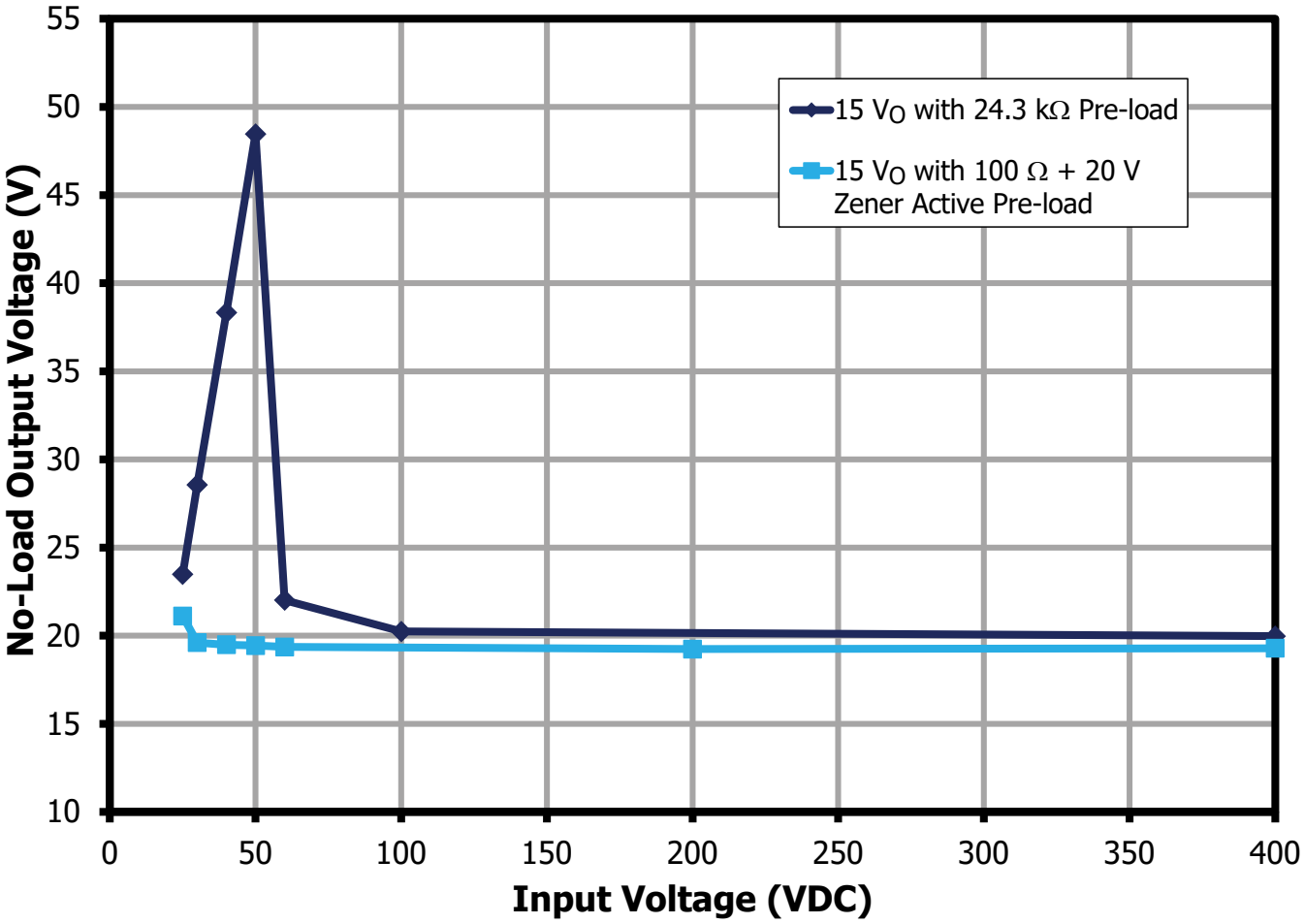


Figure 32. Buck Converter No-Load Voltage with Resistive Pre-load and Resistor-Zener Pre-load.

Revision	Notes	Date
A	Initial Release.	01/17
B	Corrected $I_{OUT(MAX)}$ and µH $I_{RMS(mA)}$ numbers in V_{OUT} column, rows 12 and 15 in Table 4.	02/19
C	Updated equation (C3) on page 16.	06/20
D	Added LNK3207, LNK3208, LNK3209 part information and Appendix D section.	09/22

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