1SP0351V2xxC
SCALE™-2 Family

Gate Driver for 4500 V Press Pack IGBT Modules
Optical I/O Interface

Product Highlights

Highly Integrated, Compact Footprint

- Ready-to-use gate driver solution for 4500 V Press Pack IGBT power modules
- Single channel gate driver
- Optical I/O interface
- Up to 1.8 W output power at maximum ambient temperature
- ±50 A peak output gate current
- -40 °C to 85 °C operating ambient temperature

Protection / Safety Features

- Short-circuit protection
- Dynamic Advanced Active Clamping (DA²C)
- Undervoltage lock-out (UVLO) protection for secondary-side (high voltage side)
- Applied double sided conformal coating

Full Safety and Regulatory Compliance

- 100% production partial discharge and HIPOT test of transformer
- Clearance and creepage distances between primary and secondary sides meet requirements for basic isolation according to IEC 61800-5-1
- RoHS compliant

Applications

- VSC-HVDC
- FACTS
- Medium Voltage Drives
- Railway Main Inverters

Description

The plug-and-play 1SP0351V2xxC gate drivers are compact single-channel intelligent gate drivers designed for the operation of 4500 V Press Pack IGBT power modules.

They feature fiber optic interface and built-in DC/DC power supply with basic isolation. Enhanced level of protection is provided by implemented short-circuit monitoring.

Power Integrations' Dynamic Advanced Active Clamping allows an extended DC-link voltage range in IGBT off-state for up to 60 s.

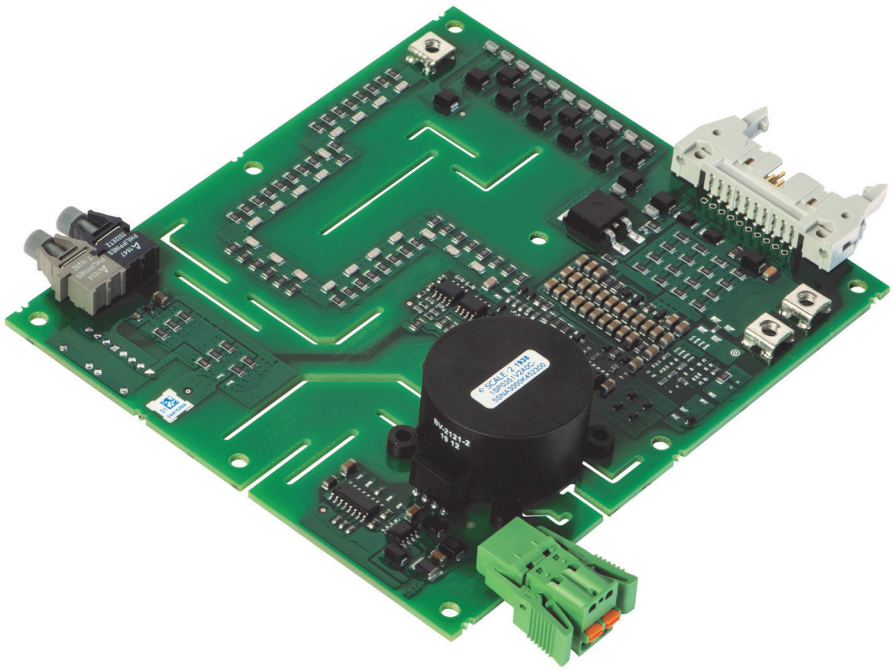

Figure 1. Product Photo of 1SP0351V2A0C.

Press Pack is a trademark of Infineon Technologies AG, Munich

Pin Functional Description

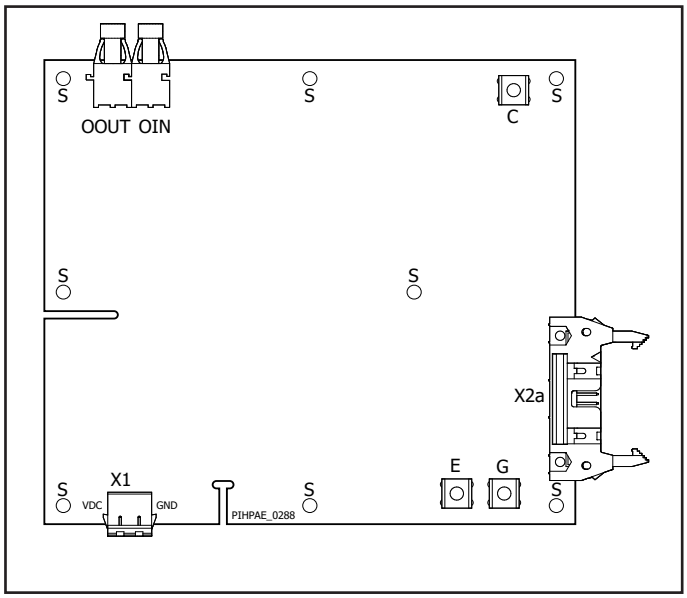

Figure 2. Pin Configuration of 1SP0351V2A0C (1SP0351V2C0C is the same as 1SP0351V2A0C but without X2a connector)

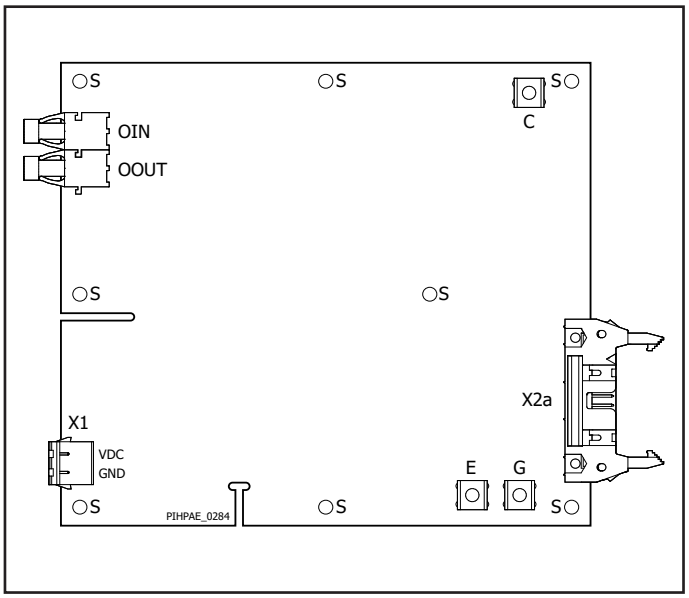

Figure 3. Pin Configuration 1SP0351V2B0C (1SP0351V2D0C is the same as 1SP0351V2B0C but without X2a connector).

Connections X1

Connections for primary-side power supply (DINKLE 2EHDRT-02P).

VDC (Pin 1)
This pin is the primary-side 15 V supply voltage connection for the integrated DC/DC converter.

GND (Pin 2)
This pin is the connection for the primary-side ground potential.

Connector X2a

AMPHENOL FCI 71922-120LF Eject Latch Header Assembly (or similar); connection to gate and emitter of IGBT module.

G (Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20)
These pins are the connection to the gate of the IGBT module.

E (Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19)
These pins are the connection to the emitter of the IGBT module.

Optical Interface

Versatile fiber optic receivers and transmitters to external controller.

OIN
This is the optical receiver (Broadcom HFBR-2522ETZ) for the command input signal.

OOUT
This is the optical transmitter (Broadcom AFBR-1529Z) for the status output signal.

Connections to Power Module

Terminal G
Gate contact of IGBT.

Terminal E
Auxiliary emitter contact of IGBT.

Terminal C
Auxiliary collector contact of IGBT.

Fixation Holes S

Holes for fixation points of stand-offs.

Note: Top and side views drawings of 1SP0351V2A0C, 1SP0351V2B0C, 1SP0351V2C0C and 1SP0351V2D0C are provided in the last pages of this datasheet.

Functional Description

The 1SP0351V2xxC is a single channel plug-and-play gate driver for Press Pack IGBT modules. It is available in different variants, which provide basic isolation between primary-side and secondary-side. The main difference between the gate driver versions is the orientation of the interface connectors which are demonstrated in the Pin Functional Description section.

The gate driver contains all necessary components for optimal and safe driving of the target power semiconductors. The driver is equipped with the following features:

- Short-circuit monitoring
- Over voltage protection to turn off the power semiconductor within the safe operation area (SOA) in case of over-current or short-circuit
- Gate clamping to reduce the effective short-circuit current
- Integrated and galvanically isolated DC/DC converter
- Fiber optic interfaces for the communication to the external controller

Power Supply (X1)
The gate driver has one VDC terminal on the interface connector X1 to supply the integrated and galvanically isolated DC/DC converter for the secondary-side. The VDC terminal must be connected to a single 15 V power supply.

The transformer of the DC/DC converter provides basic isolation according to IEC 61800-5-1 between the primary-side and secondary-side.

Undervoltage Monitoring
The secondary-side voltages are closely monitored. In case of an UVLO on the secondary-side, the fault condition will be signalized on the fiber optic status signal OOUT with a light off and the corresponding power semiconductor will be turned off.

Fiber Optic Receiver OIN
This is the edge-triggered command input signal to drive attached power semiconductor. A light signal at the input OIN will turn-on the gate of the power semiconductor. Accordingly, no light signal will turn-off the gate.

Gate driver signal is transferred from OIN to the gate with a propagation delay of $t_{P(LH)}$ for the turn-on and $t_{P(HL)}$ for the turn-off commands.

Fiber Optic Transmitter OOUT
During normal operation (i.e. the driver is supplied with power at nominal voltage, and there is no fault on the corresponding channel), the status feedback is given by a "light on" at the optical link. A fault condition is signaled by a "light off ".

The status output provides acknowledge information for every switching command by turning off the light for a duration of t_{ACK} after a delay of $t_{D(ACK)}$ referred to the edge of the received light signal on OIN. Figure 4 illustrates the timing of the fiber optic interface under normal operating conditions.

In case of a detected undervoltage lock-out condition (UVLO) on the secondary-side, the corresponding status feedback light OOUT is set to OFF as long as the UVLO condition is present. During fault condition no gate signal is transmitted to the gate driver.

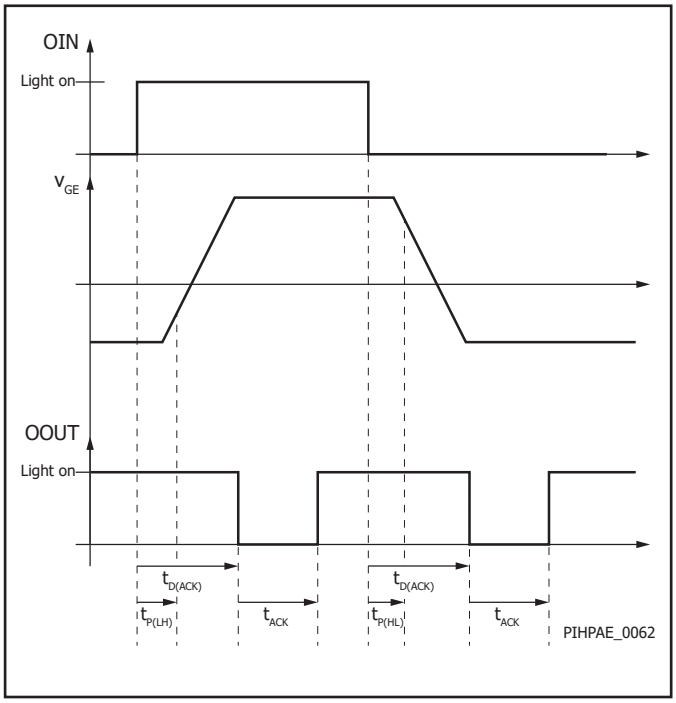

Figure 4. Fiber Optic Feedback in normal operation mode.

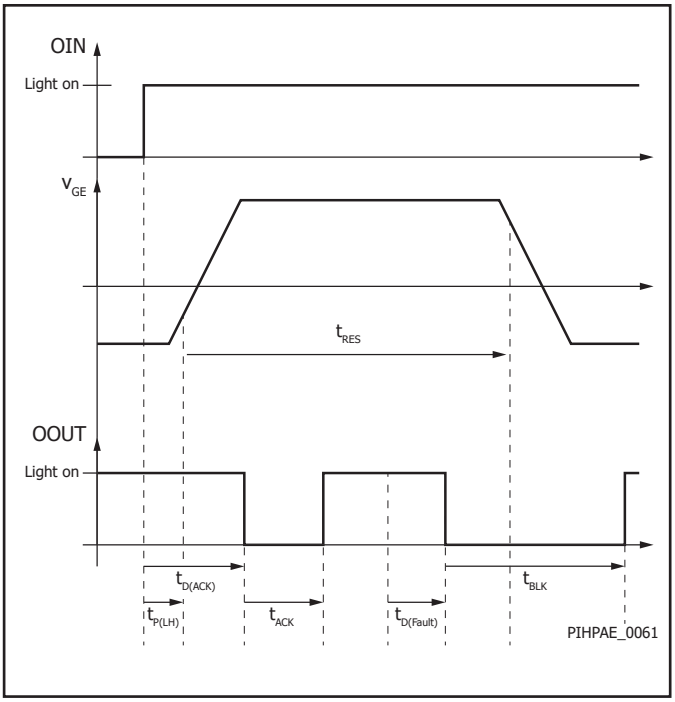

Figure 5. Fiber Optic Feedback in fault (short-circuit) operation mode.

Gate Voltage

1SP0351V2xxC possesses a voltage regulator for the positive (turn-on) rail of the gate voltage. Internal current sources are regulating actively the positive gate-emitter voltage independently of actual load conditions within the maximum specified ratings. Therefore, the on-state gate-emitter voltage $V_{GE(on)}$ of the power semiconductor equals in steady state the positive supply voltage V_{ISO}.

The off-state gate-emitter voltage $V_{GE(off)}$ equals in steady state the voltage V_{COM}. This voltage is load-dependent. It has its lowest value under no-load conditions and is increasing slightly (i.e. getting less negative) with increasing load.

In the event of an undervoltage lock-out condition the gate driver changes the control of the positive rail towards control of the negative rail V_{COM}. By this potential parasitic turn-on events of the power semiconductor are avoided.

Short-Circuit Protection

The 1SP0351V2xxC gate driver uses the semiconductor's desaturation effect to detect short-circuits.

The desaturation is monitored by using a resistor/capacitor sensing network. The collector-emitter voltage is checked after the response time t_{RES} at turn-on to detect a short-circuit. If the voltage is higher than the programmed threshold voltage $V_{CE(SAT)}$, the driver detects a short-circuit condition. The monitored power semiconductor is switched off immediately and a fault signal is transmitted to the optical status output OOUT. The light goes OFF after a delay of $t_{D(Fault)}$. Figure 5 illustrates the timing of the fiber optic interface in a short-circuit condition.

Note: The desaturation function is for short-circuit detection only and cannot provide over-current protection. However, over-current detection has a lower time priority and can be easily provided by the application.

Gate Clamping

In the event of a short-circuit condition, the gate voltage is increased due to the high dv_{CE}/dt between the collector and emitter terminals of the driven power semiconductor. This dv_{CE}/dt drives a current through the Miller-capacitance (capacitance between the gate and collector) and charges the gate capacitance, which eventually leads to a gate-emitter voltage larger than the nominal gate-emitter turn-on voltage. In consequence, the short-circuit current is increased due to the transconductance of the power semiconductor. To ensure that the gate-emitter voltage stays close to the nominal turn-on voltage, the gate driver features a gate-clamping circuitry. The gate clamping provides a voltage similar to V_{ISO} to the gate, i.e. 15 V. As the effective short-circuit current is a function of the gate-emitter voltage, the short-circuit current is limited. As consequence, the energy dissipated in the power semiconductor during the short-circuit event is reduced, leading to a junction temperature within the short-circuit safe operating area (SCSOA) limits and enabling a safe turn-off of the device.

Dynamic Advanced Active Clamping (DA²C)

Active clamping is a technique designed to partially turn on the power semiconductor in case the collector-emitter voltage exceeds a predefined threshold. The power semiconductor is then kept in linear operation. Basic active clamping topologies implement a single feedback path from the power semiconductor collector through transient voltage suppressor (TVS) diodes to the power semiconductor gate. The gate driver 1SP0351V2xxC contains Power Integrations' Dynamic Advanced Active Clamping (DA²C) that operates as follows:

When active clamping is activated, the turn-off MOSFET for the gate driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature is called as Advanced Active Clamping (AAC). The principle of AAC is illustrated in Figure 6.

Additional TVS diodes are added in series with the TVS diodes required to withstand the maximum DC-link voltage during switching. These TVS diodes are short-circuited during the IGBT on-state for about 15 to 20 µs after the turn-off command is received to ensure efficient active clamping. After this delay, these additional TVS diodes are activated and allow the DC-link voltage to be increased to a higher value during the IGBT off-state. This feature together with Advanced Active Clamping – is called Dynamic Advanced Active Clamping (DA²C). Note that the time that the voltage can be applied above the value for switching operation should be limited to short periods (<60s).

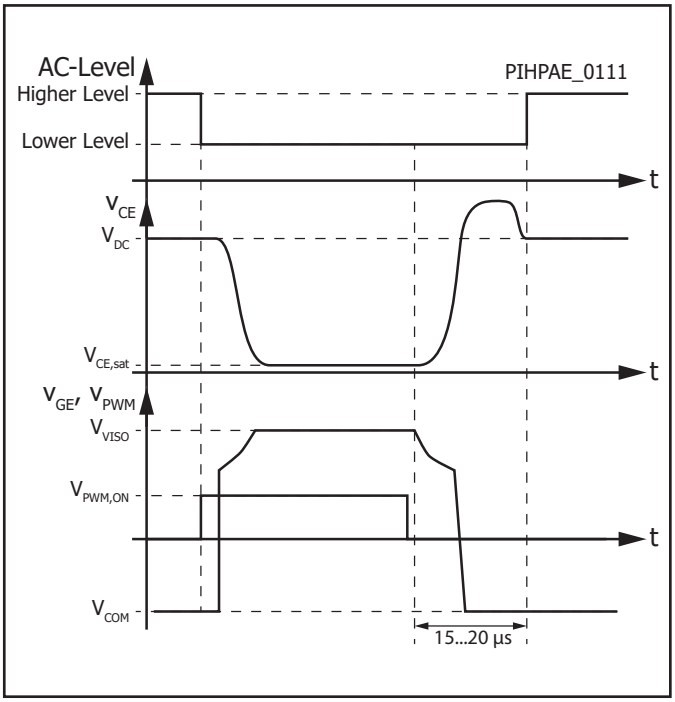

Figure 6. Dynamic Advanced Active Clamping (DA²C).

Absolute Maximum Ratings

Parameter	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Max	Units
Absolute Maximum Ratings[1]					
Primary-Side Supply Voltage	V_{DC}	VDC to GND	0	16	V
Primary-Side Supply Current	I_{DC}	Average supply current at full load		360	mA
Switching Frequency[2]	f_{SW}			2	kHz
Output Power	P_G			1.8	W
Operating Voltage	V_{CE}			4500	V_{PEAK}
DC-Link Voltage	$V_{DC\text{-}Link}$	Switching operation[3]		3400	V_{DC}
		Off State[4]		4000	
Test Voltage Primary-Side to Secondary-Side	$V_{ISO(PS)}$	50 Hz, 60 s		10200	V_{RMS}
Storage Temperature[5]	T_{ST}		-40	50	°C
Operating Ambient Temperature	T_A		-40	85	°C
Surface Temperature[6]	T			125	°C
Relative Humidity	H_R	No condensation		93	%
Altitude of Operation[7]	A_{OP}			2000	m

Recommended Operating Conditions

Parameter	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V_{DC}	VDC to GND	14.5	15	15.5	V

Characteristics

Parameter	Symbol		Conditions V_{VDC} = 15 V, T_A = 25 °C	Min	Typ	Max	Units
Power Supply							
Supply Current	I_{DC}		Without load		150		mA
			$P_G = P_{G,max}$		280		
Power Supply Monitoring Threshold (Secondary Side)	$UVLO_{VISO}$	Referenced to E	Clear fault (resume operation)	11.6	12.6	13.6	V
			Set fault (suspend peration)	11.0	12.0	13.0	
			Hysteresis	0.35			
	$UVLO_{COM}$		Clear fault (resume operation)		-5.15		V
			Set fault (suspend peration)		-4.85		
			Hysteresis		0.3		
Output Voltage (Secondary Side)	$V_{VISO-COM}$		Without load		24.4		V
			$P_G = P_{G,max}$		24.1		
Coupling Capacitance	C_{io}		Primary-side to secondary-side		8		pF
Gate Output							
Gate Turn-on Voltage	$V_{GE(on)}$		Without load		15		V
			$P_G = P_{G,max}$		15		
Gate Turn-off Voltage	$V_{GE(off)}$		Without load		-9.4		V
			$P_G = P_{G,max}$		-9.1		
Timing Characteristics							
Turn-On Delay	$t_{P(LH)}$	OIN to 50% of $V_{GE(on)}$, no load attached, optical cable length 1 m			100		ns
Turn-Off Delay	$t_{P(HL)}$	OIN to 50% of $V_{GE(off)}$, no load attached, optical cable length 1 m			125		ns
Propagation Delay of Fault State Condition	$t_{D(Fault)}$	OIN-Light ON/OFF to OOUT-Light OFF, optical cable length 1 m			100		ns
Turn-Off Delay after Fault Detection	$t_{P(HL),Fault}$				0.2		µs
Blocking Time	t_{BLK}	Delay to clear fault state			8		µs
Delay of Acknowledgment Pulse	$t_{D(ACK)}$	OIN-Light ON/OFF to OOUT-Light OFF, optical cable length 1 m			190		ns
Duration of Acknowledgment Pulse	t_{ACK}	Measured on the external controller side, optical cable length 1 m		400	600	1050	ns

Characteristics (cont.)

Parameter	Symbol	Conditions T_A = 25 °C		Min	Typ	Max	Units
Short-Circuit Protection							
Static V_{CE}-Monitoring Threshold	$V_{CE(SAT)}$				680		V
Response Time	t_{RES}	10% to 90% of V_{GE}	DC-link voltage = 3400 V		8		µs
			DC-link voltage = 2800 V		8		
			DC-link voltage = 1500 V		8		
Electrical Isolation							
Test Voltage (50Hz/1s)[8]	$V_{ISO(PS)}$	Primary to secondary side		10200			V_{RMS}
Partial Discharge Extinction Voltage[9]	PD_{P-S}	Primary to secondary side		3818			V_{RMS}
Creepage Distance	CPG_{P-S}	Primary side to secondary side, on the PCB, material group IIIa		45			mm
Clearance Distance	CLR_{P-S}	Primary side to secondary side		25			mm
Mounting[10]							
Connection Torque	$M_{Terminal}$	Terminals (C, G and E), M4 screw		1.8		2.1	Nm
Bending	l_{bend}	According to IPC				0.75	%

NOTES:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. This limit applies to the whole product family. The actual achievable switching frequency may be lower for specific gate driver variants and has to be validated in final system as it is additionally limited by maximum gate output power in conjunction with the maximum allowed surface temperature.
3. This limit is due to active clamping.
4. Due to the Dynamic Active Advanced Clamping Function (DA²C) implemented on the driver, the DC link voltage can be increased in the off state condition (e.g. after emergency shutdown). This value is only valid when the IGBTs are in the off state (not switching). The time during which the voltage can be applied should be limited to short periods (< 60 seconds).
5. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85°C.
6. The component surface temperature, which may strongly vary depending on the operating condition, must be limited to the given value to ensure long-term reliability of the product.
7. Operation above this level requires a voltage derating to ensure proper isolation coordination.
8. The transformer of every production sample has undergone 100% testing at the given value for 1s.
9. Partial discharge measurement is performed on each transformer.
10. Refer to the data sheet of the IGBT module.

Product Dimensions

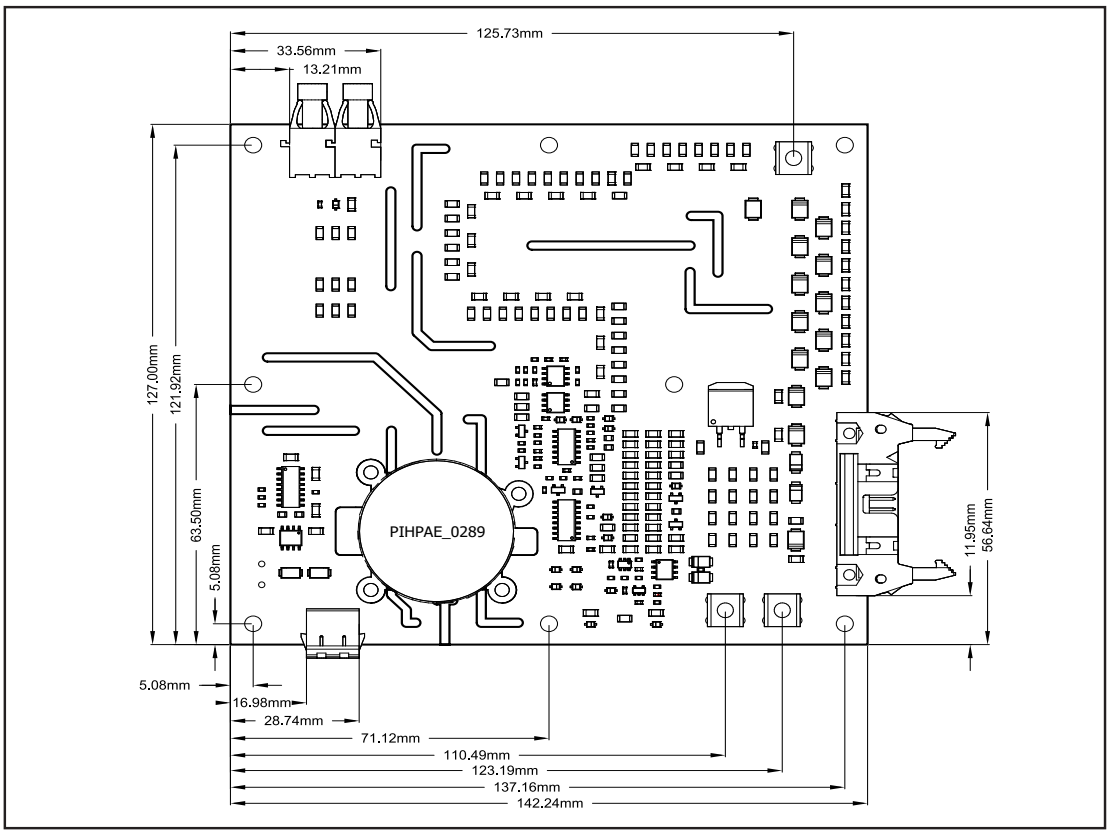

Figure 7. Top View of 1SP0351V2A0C.

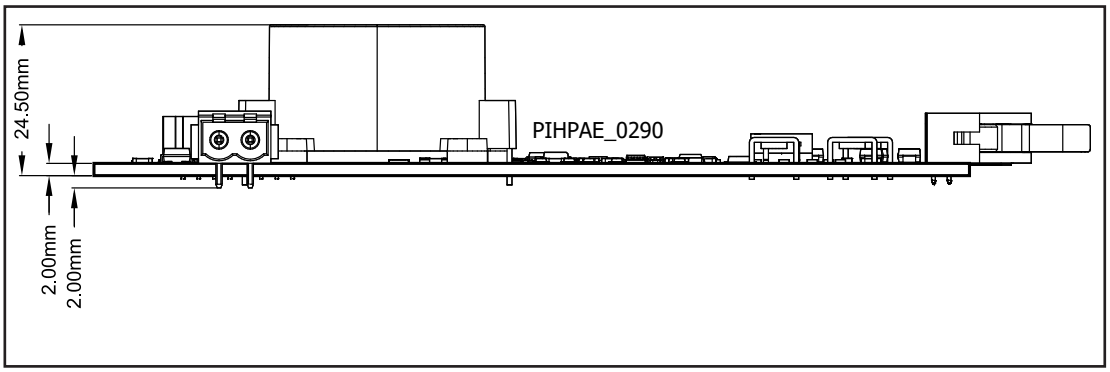

Figure 8. Side View of 1SP0351V2A0C.

Product Dimensions

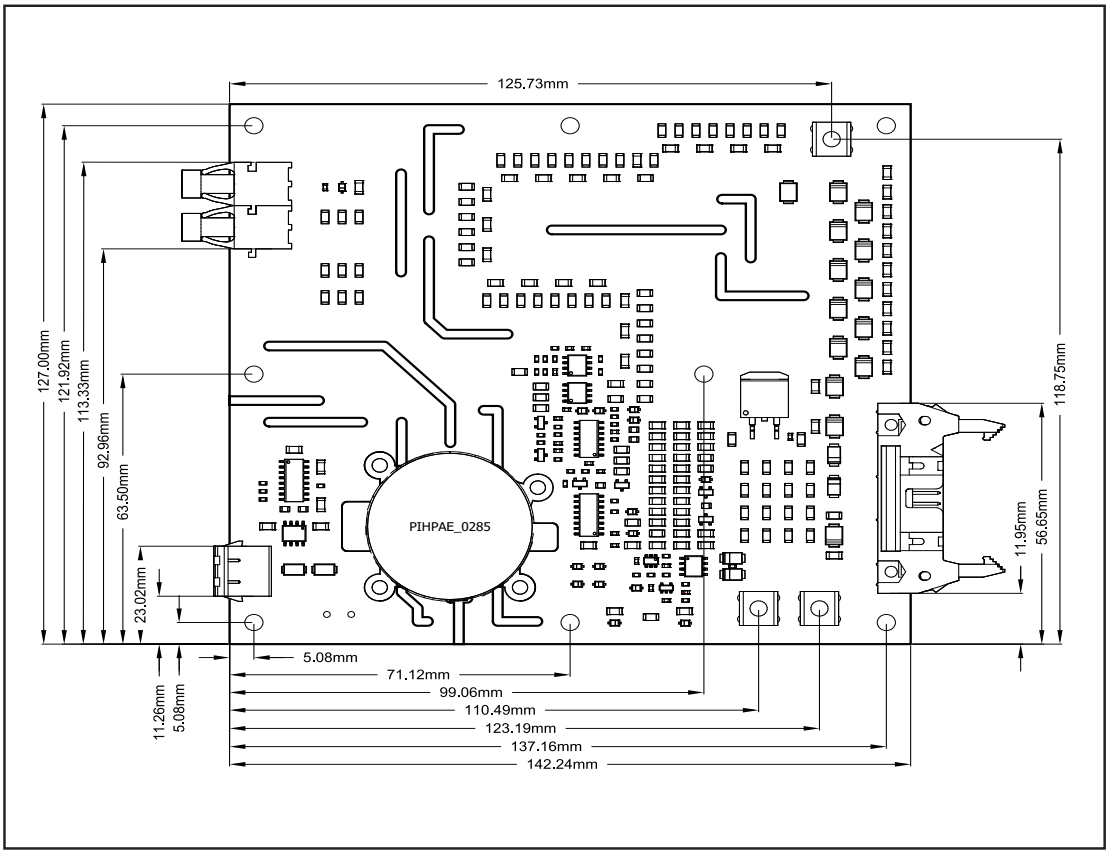

Figure 9. Top View of 1SP0351V2B0C.

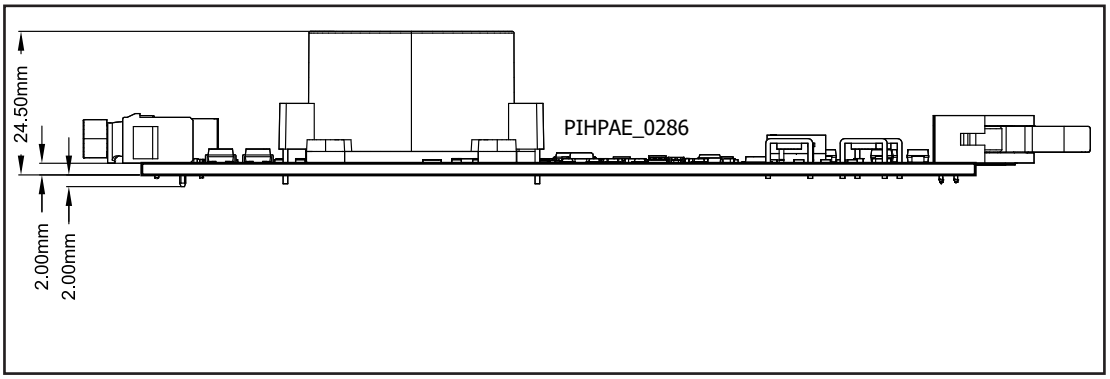

Figure 10. Side View of 1SP0351V2B0C.

Product Dimensions

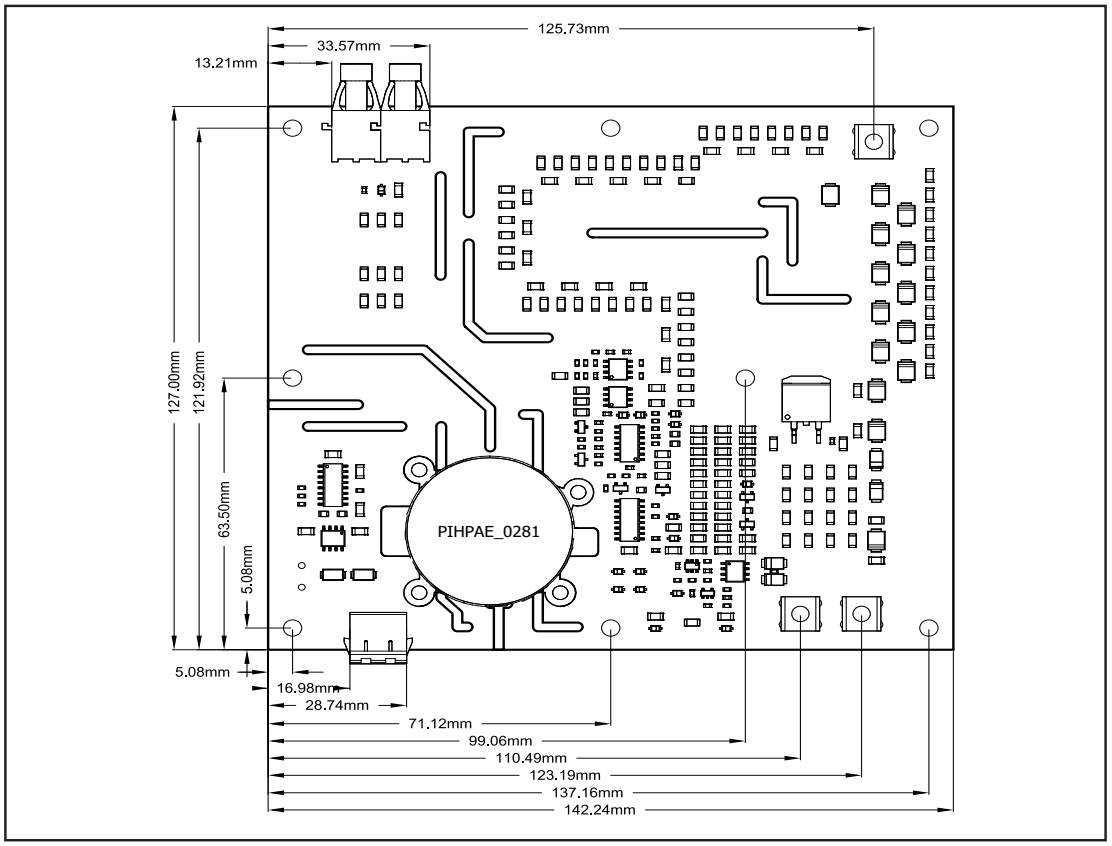

Figure 11. Top View of 1SP0351V2C0C.

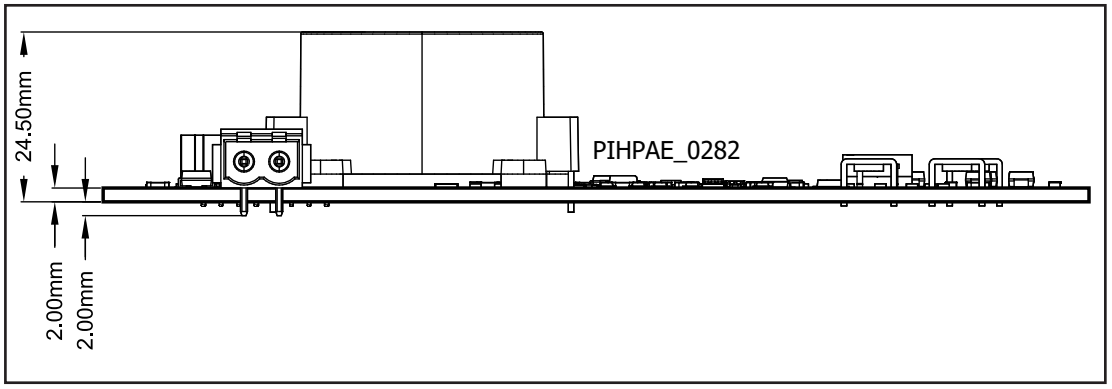

Figure 12. Side View of 1SP0351V2C0C.

Product Dimensions

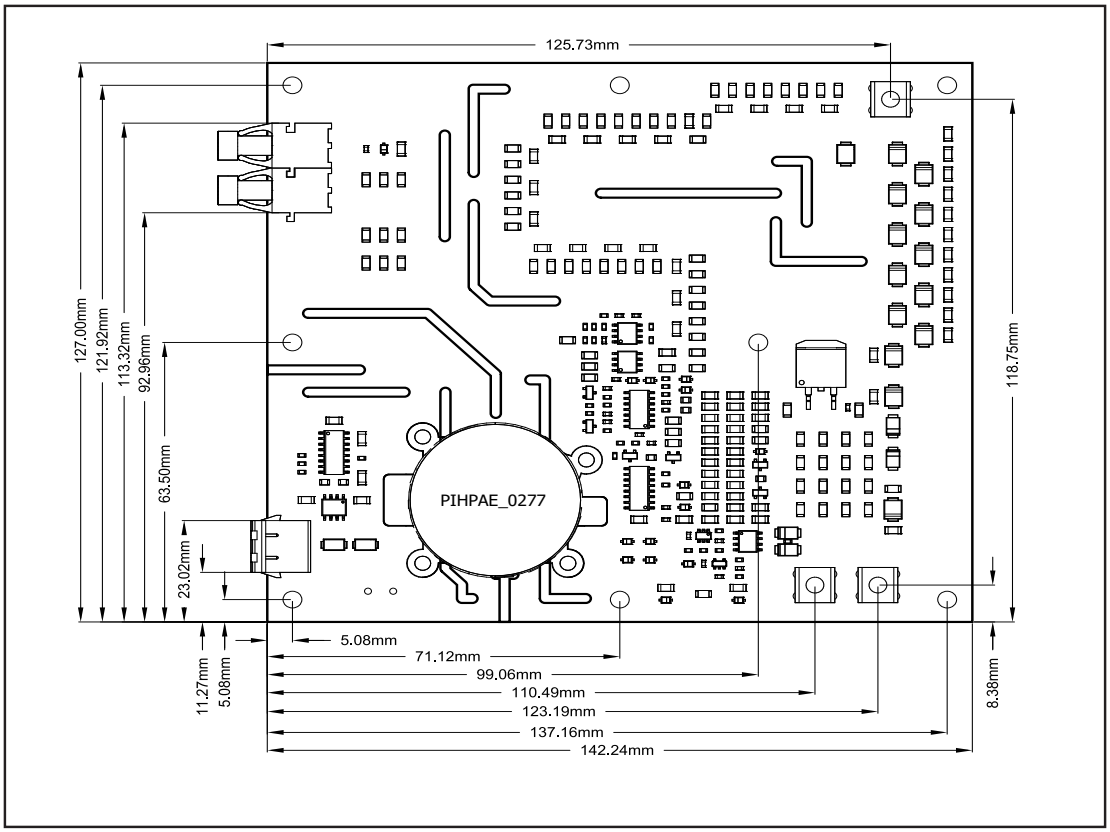

Figure 13. Top View of 1SP0351V2D0C.

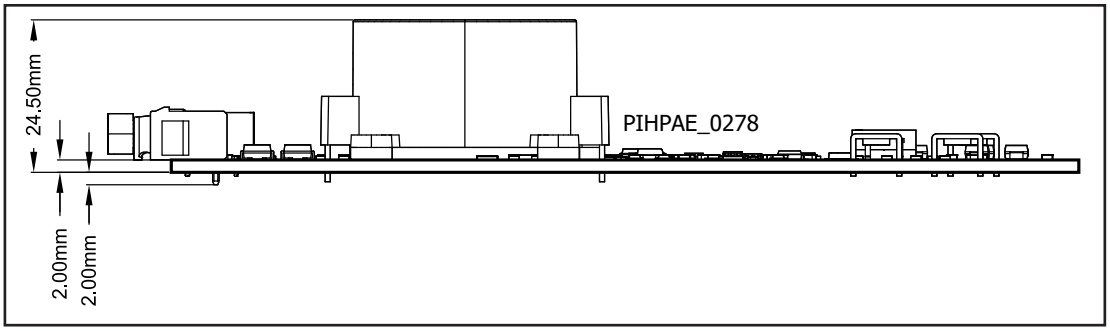

Figure 14. Side View of 1SP0351V2D0C.

Conformal Coating

The electronic components of the gate driver are protected by a layer of acrylic conformal coating with a typical thickness of 50 µm using ELPEGUARD SL 1307 FLZ/2 from Lackwerke Peters on both sides of the PCB. This coating layer increases the product reliability when exposed to contaminated environments.

Note: Standing water (e.g. condensate water) on top of the coating layer is not allowed as this water will diffuse over time through the layer. Eventually, it will form a thin film of conducting nature between PCB surface and coating layer, which will cause leakage currents. Such currents may lead to a disturbance of the performance of the gate driver.

Transportation and Storage Conditions

For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

We hereby confirm that the product supplied does not contain any of the restricted substances according to Article 4 of the RoHS Directive 2011/65/EU in excess of the maximum concentration values tolerated by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.

Reliability and EMC Qualifications Items

Test Item	Test Methods and Conditions
Environmental Tests	
Dry heat	IEC 60068-2-2, 85 °C (48 h, 2 h recovery, operated after 0.5 h)
Cold	IEC 60068-2-1, -40 °C (48 h, 2 h recovery, operated after 0.5 h)
Damp heat, steady state	IEC 60068-2-78, 65 °C (95 % RH, 24 h), 10 cycles
Damp heat cyclic	IEC 60068-2-30, 25 °C / 60 % RH, within 1 h up to 95 % RH; within 3 h up to 60 °C; stable 93 % RH for 12 h; within 3 h down to 25 C, humidity to 95 %: end at 24 h, 6 cycles
Salt spray	IEC 60068-2-11, 5 % concentration, 35 °C, 48 h
Thermal cycling	IEC 60068-2-14, -40 °C and 85 °C, ramp: 5 °C/min, dwell: 30 min, DUT operated, 100 cycles
Endurance Tests	
High temperature operating lifetime	IEC 60068-2-2, 85 °C, test duration 1000 h, DUT operated
Damp heat	IEC 60068-2-78, 85 °C / 85% R.H., 56 d, DUT operated
Thermal cycling	IEC 60068-2-14, -40 °C, 125 °C (5 K/min, 500 cycles, DUT unpowered)
EMC Tests	
Electrostatic discharge immunity	IEC 61000-4-2, contact discharge 8 kV, air discharge 15 kV, terminal test points C, E, G and GND
Radiated noise immunity	IEC 61000-4-3, frequency range 80 - 3000 MHz, sine wave, AM modulated (1 kHz), 30 V/m
	IEC 61000-4-3, frequency points 80 / 160 / 380 / 450 / 900 MHz, sine wave 80% AM modulated (1 kHz), 30 V/m, test duration 15 s per frequency point
Fast transient burst immunity	IEC 61000-4-4, capacitive clamp with 50 Ω termination, ±5 kV, 5 kHz (15 ms) and 100 kHz (0.75 ms), test points VDC and GND / C and E with attached power semiconductor, test duration 200 s
Surge immunity	IEC 61000-4-5, Power port ± 0.5 kV, collector to emitter with + 4 kV
Conducted noise immunity	IEC 61000-4-6, frequency range 0.15 – 80 MHz, sine wave 80% AM modulated (1 kHz), 20 V_{RMS}, test points VDC and GND
Magnetic field immunity	IEC 61000-4-8, 100 m/A (30 s), 1000 A/m (1 – 3 s), 3 axis
	IEC 61000-4-9, 1000 A/m, 5 cycles, 3 axis
	IEC 61000-4-10, 100 A/m, 100 kHz and 1 MHz, 3 axis, test duration 2s
Ring wave immunity	IEC 61000-4-12, line-to-line 2 kV, line-to-ground 4 kV, test points VDC and GND
Damped oscillatory wave immunity	IEC 61000-4-18, common mode 2 kV, differential mode 1 kV, 100 kHz and 1 MHz, test points VDC and GND
Transverse electromagnetic (TEM) waveguides immunity	IEC 61000-4-20, 0.08 – 1 GHz, 80 V/m, 2s
Radiated disturbances	EN 55032:2015 (CISPR32:2015)
Mechanical Tests	
Mechanical vibrations (sinusoidal)	IEC 60068-2-6, frequency range 10 - 150 Hz (7.5 mm displacement, 20 m/s², 30 min), 3 axis, 20 sweep cycles

Product details

Part Number	Power Module	Voltage Class	Current Class	Package	IGBT Supplier	$R_{G(on)}$	$R_{G(off)}$	C_{GE}
1SP0351V2A0C-5SNA3000K452300	5SNA3000K452300	4500 V	3000 A	StakPak	Hitachi Energy	1.5 Ω	7.0 Ω	330 nF
1SP0351V2A0C-5SNA2000K452300	5SNA2000K452300	4500 V	2000 A	StakPak	Hitachi Energy	1.875 Ω	8.5 Ω	330 nF
1SP0351V2B0C-5SNA3000K452300	5SNA3000K452300	4500 V	3000 A	StakPak	Hitachi Energy	1.5 Ω	7.0 Ω	330 nF
1SP0351V2B0C-5SNA2000K452300	5SNA2000K452300	4500 V	2000 A	StakPak	Hitachi Energy	1.875 Ω	8.5 Ω	330 nF
1SP0351V2C0C-P2000DL45X168	P2000DL45X168	4500 V	2000 A	Press Pack	Infineon	1.25 Ω	4.875 Ω	330 nF
1SP0351V2C0C-T2000BB45G	T2000BB45G	4500 V	2000 A	Press Pack	IXYS	2.75 Ω	15.0 Ω	220 nF
1SP0351V2C0C-TG2000SW45ZC-P200	TG2000SW45ZC-P200	4500 V	2000 A	Press Pack	CRRC	2.5 Ω	8.5 Ω	330 nF
1SP0351V2D0C-P2000DL45X168	P2000DL45X168	4500 V	2000 A	Press Pack	Infineon	1.25 Ω	4.875 Ω	330 nF
1SP0351V2D0C-T2000BB45G	T2000BB45G	4500 V	2000 A	Press Pack	IXYS	2.75 Ω	15.0 Ω	220 nF
1SP0351V2D0C-TG2000SW45ZC-P200	TG2000SW45ZC-P200	4500 V	2000 A	Press Pack	CRRC	2.5 Ω	8.5 Ω	330 nF

Revision	Notes	Date
A	Final Datasheet.	02/23

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Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji Nan
8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

Germany (Gate Driver Sales)
HellwegForum 3
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

Japan
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com